IN THE UNITED STATES DISTRICT COURT

FOR THE WESTERN DISTRICT OF WISCONSIN

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SEMICONDUCTOR ENERGY LABORATORY CO., LTD.,

Plaintiff,

v.

SAMSUNG ELECTRONICS CO., LTD., S-LCD CORPORATION, SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA, LLC and SAMSUNG MOBILE DISPLAY CO., LTD.,

Defendants.

OPINION AND ORDER

09-cv-01-bbc

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In this patent infringement lawsuit, plaintiff Semiconductor Energy Laboratory Company, Ltd. contends that certain liquid crystal display products made by defendants Samsung Electronics Company, Ltd., S-LCD Corporation, Samsung Electronics America, Inc., Samsung Telecommunications America, LLC and Samsung Mobile Display Co., Ltd. infringe four of plaintiff's patents relating to thin-film transistors: U.S. Patents Nos. 6,900,463 (the '463 patent), 7,215,402 (the '402 patent), 7,394,516 (the '516 patent) and

7,413,937 (the '937 patent). Defendants have filed counterclaims, alleging that the patents-in-suit are invalid and they have asserted several affirmative defenses.

Before the court are the parties' cross motions for partial summary judgment on plaintiff's claims that the accused products infringe the '463 patent and on all defendants' invalidity, patent prosecution laches and inequitable conduct defenses regarding the four patents-in-suit. Dkt. ##201 and 202. This opinion addresses only the parties' arguments with respect to infringement of the '463 patent and to invalidity as it relates to anticipation and obviousness only. The parties' motions on defendants' remaining defenses, including invalidity of the '463 patent for inequitable conduct and the invalidity of the asserted claims of the '402, '516 and '937 patents as anticipated or rendered obvious, will be the subject of a separate opinion.

With respect to infringement of the '463 patent, defendants have moved for summary judgment on all 14 asserted claims; plaintiff seeks summary judgment on claims 1 and 5. Defendants' motion for summary judgment on noninfringement of the '463 patent will be denied. Plaintiff's motion for summary judgment on infringement is denied in part and granted with respect to the following questions:

1. Whether the accused products satisfy the requirement in claims 1-7 and 12-13 that the channel region be "in contact" with the source and drain regions;

2. Whether the accused products satisfy the requirement in claims 1, 5, 12 and 13 that the accused channel region be located "between" the source and drain regions;

3. Whether the accused products satisfy the element of claims 8, 9, and 14 requiring the claimed thin film transistor to have "a semiconductor film having at least a source, drain and channel region";

4. Whether the accused products satisfy the requirement in claims 1-4, 8-12 and 14 that the channel region form junctions with the source and drain regions; and

5. Whether the accused products satisfy the non-single crystal semiconductor element of claims 1 and 5.

Plaintiff's motion for summary judgment will be denied with respect to the other elements of claims 1-14 of the '463 patent because material issues of fact remain in dispute. To be specific, it will be left to the jury to determine whether the accused products satisfy the requirements in claims 5 and 13 that the channel region (1) forms PI or NI junctions with the source and drain regions and (2) is comprised of an intrinsic amorphous silicon semiconductor material.

With respect to invalidity of the '463 patent, defendants base their motion for summary judgment on their assertions that the asserted claims are anticipated or rendered obvious by Sakamoto, rendered obvious in light of Matsumura and LeComber and rendered obvious in light of Matsumura and Sakamoto. Plaintiff has moved for summary judgment

on defendants' claims that the '463 patent claims are anticipated by Sakamoto, Kazmerski and JP '663 and '664.

The material issues of fact in dispute about whether Sakamoto discloses the "recombination center neutralizer" and "intrinsic channel region" elements of the '463 patent prevent me from deciding as a matter of law whether Sakamoto anticipates the '463 patent or renders it obvious. Therefore, I will deny the parties' motions for summary judgment on those issues. For the same reason, I will deny defendants' motion for summary judgment on the obviousness of the '463 patent in light of Matsumura and LeComber or Sakamoto. In light of the parties' factual disputes relating to obviousness, I decline to address plaintiff's arguments of secondary obviousness considerations.

Plaintiff's motion for summary judgment will be granted with respect to defendants' claim that the '463 patent is invalid as anticipated by Kazmerski because defendants have failed to show that it would have been obvious to combine two different embodiments appearing in that reference. Plaintiff's motion for summary judgment on defendants' claim that the '463 patent is invalid as anticipated by JP '663 and '664 will be denied. The following questions remain to be decided at trial:

1. Whether the '463 patent is anticipated or rendered obvious by Sakamoto;

2. Whether JP '663 and '664 anticipates the '463 patent; and

3. Whether the combination of Matsumura and LeComber or Matsumura and Sakamoto render the '463 patent claims obvious;

For the purpose of deciding the parties' motions for summary judgment on infringement and invalidity of the '463 patent, I find that the following facts are undisputed and material.

UNDISPUTED FACTS

A. The Parties

Plaintiff Semiconductor Energy Laboratory Co. Ltd. is a Japanese corporation. Defendants Samsung Electronics Company, Ltd., S-LCD Corporation and Samsung Mobile Display Co., Ltd. are Korean corporations. Defendants Samsung Electronics America, Inc. and Samsung Telecommunications America, LLC are American corporations. Defendants manufacture a large number of consumer electronic products that include televisions, laptop computers, computer monitors and cell phones. Until 2005, defendants manufactured thin film transistors under an express written license with plaintiff.

B. General Technology

Liquid crystal displays (LCD) modules or panels, including those in the accused products, incorporate thin film transistors containing amorphous silicon semiconductor material. Each LCD is divided into thousands (or millions) of tiny picture elements called

"pixels," which form the image on the LCD screen. Increasing the number of pixels in a given area produces a higher resolution picture. A high-definition LCD has more pixels than a standard-definition screen of the same size. The color and brightness of each pixel is determined by even smaller elements in the LCD called sub-pixels, each of which is associated with a thin film transistor that works as an electronic switch.

An LCD is a multilayered "sandwich" consisting of at least a backlight, a thin film transistor substrate, liquid crystal material, a counter substrate, a seal, and driver circuitry. The **backlight** is the LCD's light source. A **thin film transistor substrate** contains an array of thousands of thin film transistors that work as electric "switches" to control the electric current going to each individual pixel. The thin film transistors effectively turn individual pixels on and off and vary the brightness and intensity of individual pixels to help create colors. **Liquid crystal material** is located between the thin film transistor substrate and the counter substrate; it affects the display of light from the backlight. A **counter substrate** is fitted with color filters that determine the colors to be displayed. Each pixel has three sub-pixels, each corresponding to a different color filter, typically, red, green and blue, on the counter substrate. The amount of light that passes through each sub-pixel determines the color of the pixel. The **seal** is an adhesive material that binds the thin film transistor and counter substrates together, enclosing the liquid crystal material and LCD components and

preventing impurities from entering the device. **Driver circuitry** is attached to or on the thin film transistor substrate and sends signals to control the thin film transistors.

Plaintiff's expert, Professor Tsu-Jae King Liu, identified the accused products by product code, module code, panel code, product ID and mask design code. The following chart generally summarizes certain Samsung manufacturing lines, facilities, panel sizes and products:

Fabrication Facility	Generation Line	Panel Size(s) (inches)	Product
Chonan	L3	10.6, 12.1, 13.3, 14, 14.1	Notebook PC
Chonan	L4	12.1, 14.1, 15, 15.4	Notebook PC
Chonan	L4	21.3, 30	Monitor
Chonan	L5	8.9, 10.1, 13.3, 13.4, 14, 15, 15.4, 15.6, 17.3	Notebook PC
Chonan	L5	15, 17, 19, 20, 24, 27	Monitor
Chonan	L6	11.6, 12.1, 13.3, 14, 14.1, 15, 15.4, 16, 17, 18.4, 19	Notebook PC
Chonan	L6	17, 18.5, 19, 20.1, 21, 22	Monitor
Tanjung	T7-1	32, 40, 46	Television
Tanjung	T7-2	17, 19, 20, 22, 23, 24, 26, 27	Monitor
Tanjung	T7-2	26, 32, 40, 46, 52, 57, 70, 82	Television
Tanjung	T8-1	18.5, 21.5, 22	Monitor
Tanjung	T8-1	21.6, 32, 46, 52, 55	Television
Tanjung	T8-2	32, 46, 52	Television

C. The '463 Patent Claims

On May 31, 2005, the '463 patent was issued to plaintiff Semiconductor Energy Laboratory Company, Ltd. for an invention entitled "Semiconductor Device," which describes the manufacturing steps of a thin film transistor. The '463 patent indicates that the patent application was filed on September 8, 1992 and claims priority to Japanese Patent

Application 55-88975 filed on June 30, 1980. It names Shunpei Yamazaki and Yujiro Nagata as inventors. The '463 patent recites the following claims:

> 1. A thin film transistor comprising:
>
> a pair of source and drain regions;
>
> a channel region between said source and drain regions; and
>
> a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween, said channel region comprising an amorphous silicon semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof;
>
> said pair of source and drain regions comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and having an impurity conductivity type to form junctions in contact with said channel region,
>
> wherein at least a portion of said gate insulating film which is in direct contact with said channel region comprises a nitride.
>
> 2. A thin film transistor according to claim 1 wherein said channel region has an intrinsic conductivity type.
>
> * * *
>
> 5. A thin film transistor comprising:
>
> a pair of source and drain regions;
>
> a channel region between said source and drain regions; and
>
> a gate electrode adjacent to said channel region with a gate insulating film

interposed therebetween,

said channel region comprising an intrinsic amorphous silicon semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof;

said pair of source and drain regions comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and having a P or N type conductivity to form PI or NI junctions in contact with said channel region,

wherein at least a portion of said gate insulating film which is in direct contact with said channel region comprises a nitride.

* * *

8. A thin film transistor comprising:

a semiconductor film having at least source, drain and channel regions comprising amorphous silicon, said source and drain regions forming junctions with said channel region;

a gate insulating film adjacent to said channel region; and

a gate electrode adjacent to said channel region with said gate insulating film therebetween,

wherein said amorphous silicon semiconductor film contains a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and at least a portion of said gate insulating film which is in contact with said channel region comprises a nitride.

9. A thin film transistor according to claim 8 wherein said channel region has an intrinsic conductivity type.

* * *

12. A thin film transistor comprising:

a pair of source and drain regions;

a channel region between said source and drain regions; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween,

said channel region comprising an amorphous silicon semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof;

said pair of source and drain regions comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and having an impurity conductivity type to form junctions in contact with said channel region,

wherein at least a portion of said gate insulating film which is in direct contact with said channel region comprises a nitride;

wherein said channel region is interposed between said gate insulating film and another insulator different from said gate insulating film; and

wherein at least a portion of said junctions are covered by said another insulator.

13. A thin film transistor comprising:

a pair of source and drain regions;

a channel region between said source and drain regions; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween,

said channel region comprising an intrinsic amorphous silicon semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof;

said pair of source and drain regions comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and having a P or N type conductivity to form PI or NI junctions in contact with said channel region,

wherein at least a portion of said gate insulating film which is in direct contact with said channel region comprises a nitride; and

wherein said channel region is interposed between said gate insulating film and another insulator different from said gate insulating file; and

wherein at least a portion of said junctions are covered by said another insulator.

14. A thin film transistor comprising:

a semiconductor film having at least source, drain and channel regions comprising amorphous silicon, said source and drain regions forming junctions with said channel region;

a gate insulating film adjacent to said channel region; and

a gate electrode adjacent to said channel region with said gate insulating film therebetween,

wherein said amorphous silicon semiconductor film contains a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and at least a portion of said gate insulating film which is in contact with said channel region comprises a nitride; and

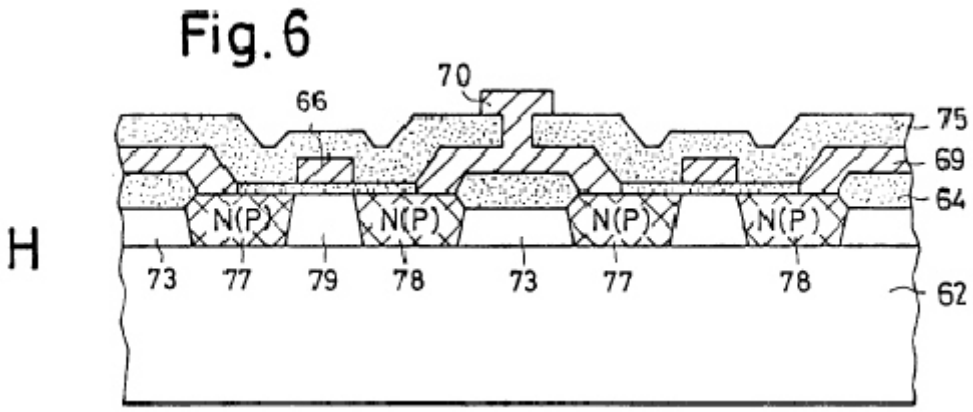
wherein said channel region is interposed between said gate insulating film and another insulator different from said gate insulating film; and

wherein at least a portion of said junctions are covered by said another insulator.

D. "Channel Region"

1. Intrinsic evidence

All of the asserted claims of the '463 patent require the "channel region" of the thin film transistor to have some contact with the source and drain regions. Independent claims 1, 5, 12, and 13 claim a "channel region between said source and drain region" and require the source and drain regions to "form junctions in contact" with the channel region. Independent claims 8 and 14 require only that the source and drain regions "form[] junctions" with the channel region. Figure 6H of the '463 patent specification depicts a thin film transistor:



Regions 77, 78 and 79 are the source, drain and channel regions, respectively, and all are made of a semi-amorphous semiconductor material. The specification does not discuss the differences between a one-layer channel region and a two-layer channel region.

2. Use of term in related patents and other extrinsic evidence

In Semiconductor Energy Laboratory Co., Ltd. v. Samsung Electronics Co., Ltd., No. 96-1460-A (E.D. Va. 1998) (SEL I), plaintiff asserted U.S. Patent No. 5,543,636 (the '636 patent) against some of the Samsung defendants in the instant case. In SEL I, the defendants argued the following with respect to the '636 patent in an April 1998 claims construction brief:

> SEL may argue that the majority of current path traverses along the channel in the I layer immediately adjacent the to [sic] interface between the gate insulator and the I-layer, and that this channel is both parallel to the substrate and between the source and drain regions. However, the claims require that the "source and drain regions [form] respective junctions with said channel region." Thus, the channel region cannot be limited to the portion of the bottom gate device through which charge carriers move roughly parallel to the substrate, but must also include those vertical areas through which charge carriers exit and enter the respective source and drain regions.

Dkt. #289, Exh. 2 at 24. The defendants also argued that "the channel region cannot be limited to the portion of the bottom gate device through which charge carriers move roughly parallel to the substrate, but must also include those vertical areas through which charge carriers exit and enter the respective source and drain regions." Id. at 23-24.

In a 2003 order construing claims in U.S. Patent No. 6,355,941 (the '941 patent), which has the same specification as the '463 patent, United States District Judge William Alsup of the Northern District of California construed "channel region" as "the area—labeled 79 of Figure 6H—between the source and drain regions through which the channel is

formed; the 'channel region' includes but is not limited to the channel and does not include the insulating layer." Semiconductor Energy Laboratory Co., Ltd. v. Acer Incorporated (Acer), No. 02-02800 (N.D. Cal. June 9, 2003), dkt. #289, Exh. 1 at 9. Judge Alsup rejected one suggestion of defendants that "channel region" be construed as "the portion of the semiconductor layer through which a channel passes or in which a channel is formed." Id. at 8-9. The parties agreed that "channel" was the "current path between the source and drain electrodes." Id. at 9.

As previously noted, the '463 patent uses the term "between" to describe the location of the channel region. Webster's Third New International Dictionary 209 (1966) defines "between" as "from one to the other of," "in the space that separates," "JOINING, CONNECTING <a passageway—two rooms>," "in an intermediate position in relation to two other objects" and "filling the space limited by two objects."

3. Accused products

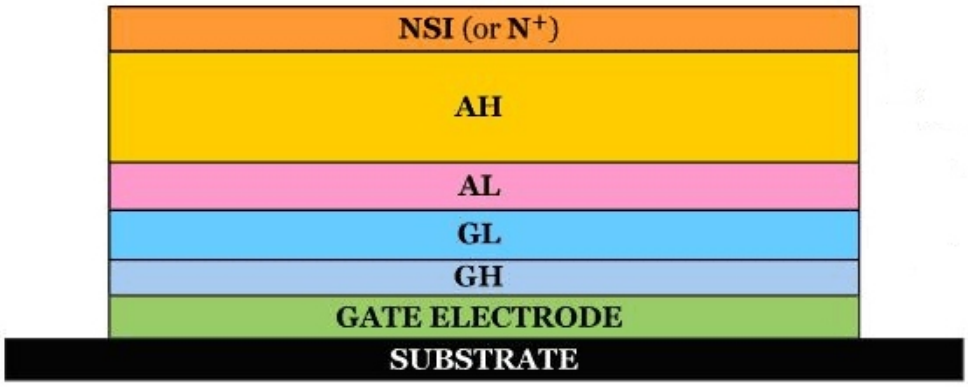
The thin film transistors in the accused products are manufactured by forming layers sequentially. The manufacturing process and conditions of the accused products are documented in two kinds of files. "Recipe files" specify the order in which the layers are formed and the compounds used to deposit each layer of material in the thin film transistors in the accused products. "Process flows" specify the overall manufacturing sequence,

including the names of the recipe files needed to manufacture the product and the order in which the recipe files are used.

The semiconductor layers in defendants' products are formed using a process called chemical vapor deposition (CVD). One example of a chemical vapor deposition recipe used in assembling the accused products from Line 2, entitled "ACTIVE," indicates that two gate insulation layers (GH and GL) are formed on top of a gate electrode. (The parties do not indicate what the initials "GH" and "GL" refer to. The parties also fail to explain what Line 2 is; however, it appears to be a specific product production line for certain accused products.) The ACTIVE recipe provides that subsequently, three layers of semiconductor material called AL, AH and either NSI (or N^+) are formed sequentially on top of the gate insulating layers. (The parties do not define what these initials stand for.)

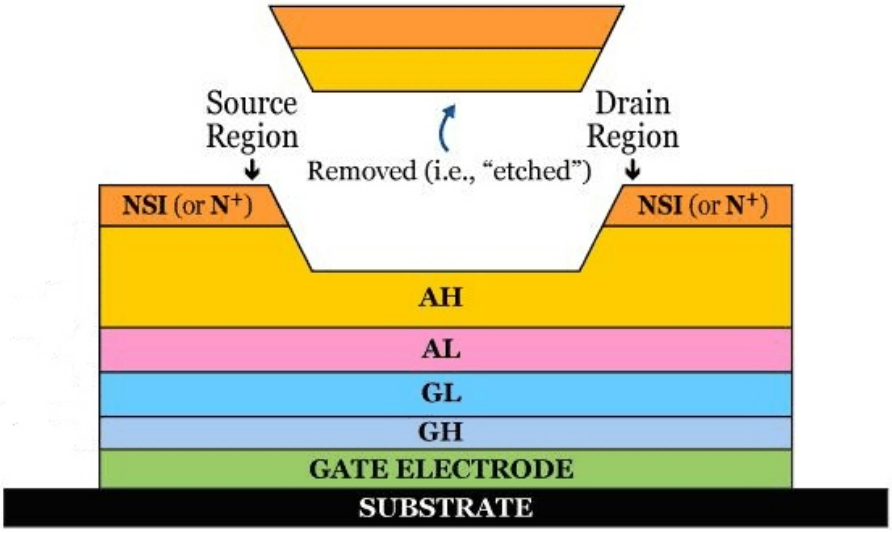
Semiconductor materials have different "conductive properties," that is, different ways in which a current travels across the material. At the time of the alleged invention of the '463 patent, people of ordinary skill in the art used the terms "N-type," "N^+-type," "P-type," "P^+-type," and "I-type" to identify the conductive properties of semiconductor materials. An interface between an N-type material and an I-type material is called "NI." An interface between an N^+-type material and and I-type material is called an N^+I. (The parties do not agree whether the interface between an N^+-type material and an I-type material can be referred to also as NI.)

The figure below illustrates the resulting thin film transistor in the accused products:



All of the accused products have AH and AL layers. (The parties disagree about the composition, purpose and function of the AH and AL layers.) Defendants' engineer, Seok Je Seong, testified that AL is one of the two steps that forms amorphous silicon; the other step is the AH. He stated that "two steps are what are needed to realize one amorphous layer, and this AH is — is the case where a faster deposition speed is realized on the layer." Dkt. #292, Exh. 55 at 184.

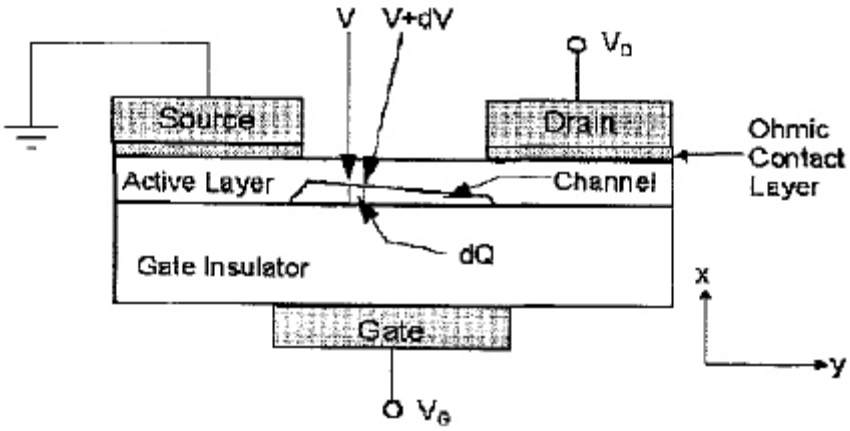
During defendants' manufacturing process, a portion of the NSI and AH layers is removed or "etched" to create separate source and drain regions in the NSI layer. The following figure illustrates this process:



The asserted '463 patent claims require the claimed source and drain regions to contain an "impurity conductivity type" (claims 1 and 12) or a "P or N type conductivity" (claims 5 and 13). The ACTIVE recipe file for Line 2 shows that the NSI layer is the only layer that contains an N-type impurity, namely phosphine (PH3). Therefore, the claimed source and drain regions of the '463 patent can be only in the NSI layer. In the accused products, the NSI layer contacts the AH layer.

In all thin film transistors, the channel is a layer of semiconductor material along the gate insulating layer that is rendered conductive by the gate electrode. When a voltage is applied to the gate electrodes of a thin film transistor, electric charge flows from the source region through the channel region to the drain region. A conductive layer of mobile electronic charge, called the channel, forms at the interface with the gate insulating layer to

electrically connect the source and drain regions. Generally, the channel region is the region where the channel forms when the thin film transistor is on. An example of this is illustrated below:



In the accused products, when the thin film transistor is off, no current flows from the source region through either the AH or AL layer to the drain region. When the thin film transistor is turned on, current flows from the source region through the AH layer to the AL layer, then back through the AH layer on its way to the drain region.

The thickness of each layer in a thin film transistor can be determined using a technique called secondary ion mass spectrometry (SIMS), which detects the concentration of an element in a solid material. Recipe files for the accused products show that the concentration of hydrogen varies in the AL, AH and NSI (or N^+) layers. The spectrometer analysis detects changes in hydrogen concentration across these layers and identifies the thickness of each layer. For example, spectrometer analysis of accused product

L2220QCFC1-TFT (from Line 2) showed that the AH layer is approximately 190 nanometers thick, the AL layer is approximately 20 nanometers thick and the NSI (or N^+) layer is approximately 50 nanometers thick. High resolution Lorentz Electron Microscopy on this product shows a thin AL layer between the AH and GL layers. Spectrometer analysis determined that in most of the accused products, the AL layer is approximately 20 nanometers thick, and in all such cases, the AL layer is at least 10 nanometers thick.

According to an article by Andrew C. Tickle, entitled Thin Film Transistors, a New Approach to Microelectronics, "[t]ypically the channel thickness in a TFT [thin film transistor] is of the order of a few tens of Angstroms." (One nanometer equals ten Angstroms.) N. Lustig and W.E. Howard explain in "Variable Range Hopping Conductivity in Hydrogenated Amorphous Silicon Thin Film Transistors," Solid State Communications, Vol. 72 (1), 59-61 (1989), that the thickness of a channel in an amorphous silicon TFT "varies from about 60 [Angstroms] to about 8.5 [Angstroms] . . . ."

There are some differences in the way the AL and AH layers perform in the accused products. Process flows show that settings called "plasma power" (shown in the recipe files as "RF POWER") and "gas flow rate" (shown in the recipe files as "SIH4") are lower for the AL layer than the AH layer. Further, a test that measures the carrier mobility, which determines how easily electrons move under an applied electric field in a material, shows that the material of the AH layer has carrier mobility three times lower than that of the AL layer.

During manufacturing of the accused products, the AH layer is deposited at a much higher rate (130 nanometers in 35 seconds) than the AL layer (10 nanometers in 19 seconds).

E. "Semiconductor Film"

1. Intrinsic evidence

a. Claim language

Claims 8 and 14 discuss a "semiconductor film having at least source, drain and channel regions." The '463 patent specification discloses a single embodiment of a thin film transistor in which the source, drain and channel regions are formed in a single layer of semiconductor material. It also states that "a non-single crystal semiconductor layer 63 is formed to a thickness of 0.3 to 1 um on the substrate 62." The '463 patent does not disclose an embodiment in which source and drain regions are in one layer of semiconductor material and a channel region is in a different layer of semiconductor material. Figure 6H of the '463 patent illustrates a thin film transistor with source region 77, drain region 78, and channel region 79, all formed in a single layer of semiconductor material.

b. Patent prosecution

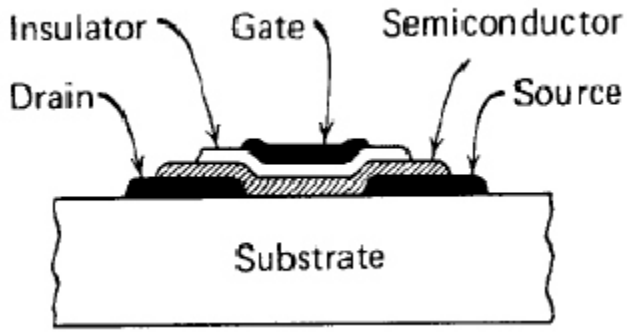
During the prosecution of the '463 patent in 1997, the patent examiner rejected pending claims of the '463 patent as obvious over the Matsumura reference in view of JP '330, Le Comber 3/79, Ovshinsky '941, and in further view of Madan 1976. The examiner

stated that "Matsumura teaches a thin film fet [field effect transistor] comprising an amorphous insulating glass substrate, an intrinsic amorphous silicon channel layer with junctions to n-type amorphous silicon source and drain regions, and a silicon dioxide gate insulating layer." Matsumura discloses a channel region located in one semiconductor layer (the "undoped I layer") and source and drain regions located in a second, separate layer above the channel layer (the "N^+ layer"). In Matsumura, the N^+ layer is located above the undoped layer. In an April 10, 1997 declaration submitted to the patent examiner, Yamazaki identified a transistor "in accordance with the present invention" that had source, drain and channel regions in a single layer of semiconductor material.

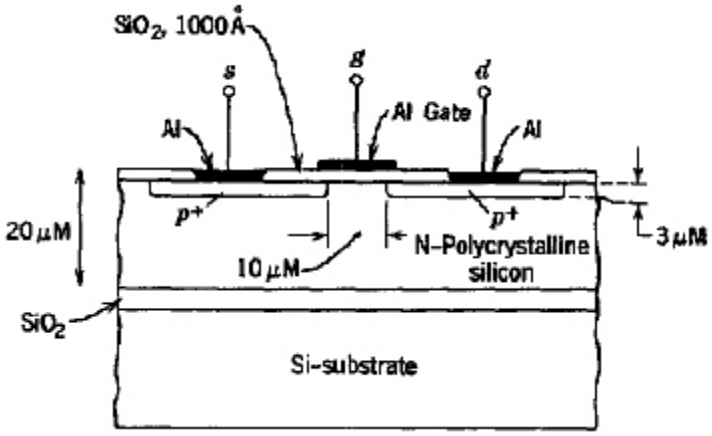
On January 14, 1999 and December 1, 1999, the examiner rejected the pending '463 patent claims again, relying this time on a number of references, including Matsumura. Nothing in the rejection letters discusses a "semiconductor film." At no point during the '463 patent prosecution did plaintiff distinguish Matsumura by claiming that the channel region was limited to channel regions on the same plane as (or co-planar with) the source and drain regions.

2. Extrinsic evidence

As of June 30, 1980, those of ordinary skill in the art knew of multiple designs for thin film transistors, including ones that have the source and drain in the same layer as the channel and ones that have the source and drain in a different layer from the channel. For example, the textbook Theory and Applications of Field-Effect Transistors (1970) by Richard S.C. Cobbold, contains the following figure, which depicts a "Weimer-Type" thin film transistor that has source and drain regions in a different layer from that containing the channel region.



(The parties do not identify which region in this figure is the "channel region.") The same textbook describes the following figure as a thin film transistor described by "Fa and Jew," which has source and drain regions labeled "p^+" in the same layer as the channel region.



(The parties do not identify which region in this figure is the "channel region.")

U.S. Patent No. 5,723,371 (the '371 patent), which is assigned to Samsung Electronics Co., Ltd., explains that "[t]he typical method of fabricating a thin film transistor . . . generally comprises the steps of forming gate electrode 2 on bare glass substrate 1; depositing gate insulating film 3 on gate electrode [2]; forming semiconductor film 6 by depositing amorphous silicon film 4 and N+ amorphous silicon film 5 sequentially; and forming source and drain electrodes 7a, 7b by depositing metal layers on semiconductor film 6."

During the prosecution of the '941 patent in 1995 (which is related to the patent-in-suit), plaintiff specifically proposed claims that recited "said transistor having at least source, drain, and channel regions formed within one semiconductor layer." The next year, plaintiff proposed "a pair of source and drain regions formed in the same layer as said channel

region." Claim 8 of the '941 patent claims "a pair of source and drain regions formed in the same layer as said channel region."

3. Accused products

The accused products do not have a single layer of semiconductor material with source, drain and channel regions. The source and drain regions are in one layer and the channel region is in a different layer. (The parties dispute whether the single layer and multiple layer designs function differently. Defendants contend that a multiple layer design insures that there are no contaminants between the source, drain and channel regions and that a single layer design requires the use of ion implantation or diffusion to form source and drain regions in the same semiconductor film, a process that degrades semiconductor materials and results in lower conductivity.)

F. "Junction"

1. Background

Claims 1, 5, 8 and 12-14 use the term "junctions" to refer to the border (or "interface") between two materials. An increase in voltage applied to an interface may result in a proportionate or a disproportionate increase in electric current across the interface. A current-voltage graph, also referred to as an I-V curve, shows the amount of electric current

across an interface for a given amount of voltage applied to the interface. An ohmic contact is a type of interface in which current flows across the interface in both directions with equal ease. The term "ohmic" describes a linear relationship between voltage and current; stated another way, a unit increase in voltage always results in the same increase in current flow through the junction. In an ohmic interface, an increase in voltage to the interface results in a proportional increase in electric current across the interface. Therefore, ohmic contacts produce substantially linear I-V curves.

The term "non-ohmic" describes a non-linear relationship between voltage and current: a unit increase in voltage results in a disproportionate or variable increase in current flow through the junction and produces a non-linear current-voltage graph. Non-ohmic interfaces also are referred to as "rectifying" interfaces. They allow current to flow easily in one direction. Rectifying junctions are non-ohmic. (The parties dispute whether non-rectifying junctions can be either ohmic or non-ohmic.)

NI, PI and PN interfaces are non-ohmic or rectifying. (The parties do not agree whether the N^+I interface between the source and drain regions and the channel region in the accused products is ohmic or non-ohmic. Defendants assert that these heavily doped interfaces are ohmic; plaintiff contends that they are rectifying or non-ohmic.)

2. Intrinsic evidence

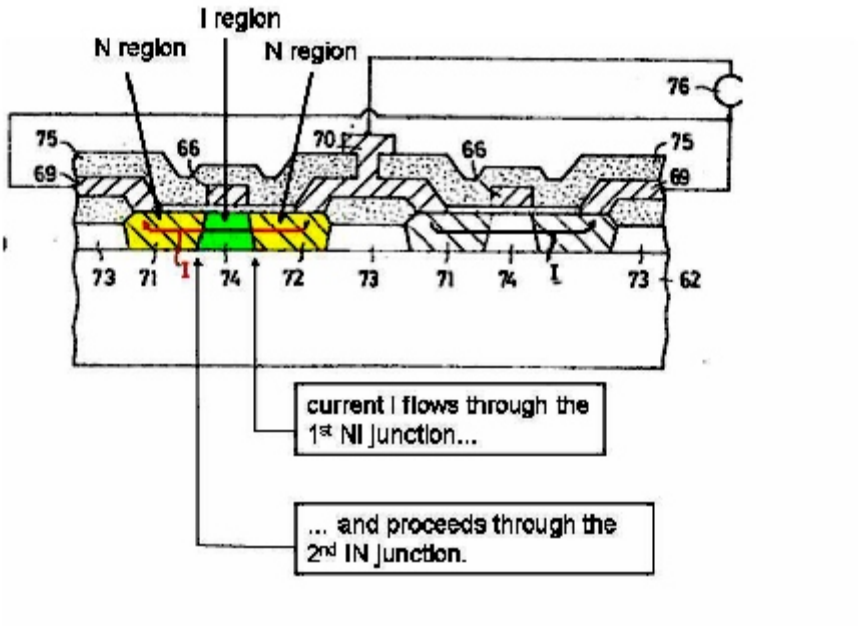
The '463 patent refers to interfaces between the source and channel semiconductor regions as "junctions" and uses the term to describe NI, PI and PN interfaces. For example, claims 5 and 13 recite "said pair of source and drain regions . . . having a P or N type conductivity to form PI or NI junctions in contact with the channel region." Similarly, the patent specification states that "it is possible to obtain various semiconductor elements . . . which have at least one of PI, PIN, PI [sic] and NI junctions." Col. 13, lns. 1-3. The '463 patent also refers to an ohmic contact, but in a different context:

> A [sic] conductive layers 69 and 70 similar to the layer 66 extending on the insulating layer 64 are formed to make ohmic contact with the semiconductor layer 63 through the windows 67 and 68, respectively.

The specification explains that layer 66 is an "amorphous or semiamorphous semiconductor . . . doped with 0.1 to 5 mol % of an N type conductive material." (The parties do not agree whether a person of ordinary skill in the art would have considered this type of material to be only N^+ or also N-type. Because layer 63 does not contain any impurities, it is an I-type. Therefore, the parties also dispute whether a person of ordinary skill in the art would have understood about layers 69 and 70, that is, whether they form an N^+I ohmic contact or whether they form NI or N+I junctions with layer 66.)

Figure 6G of the patent specification illustrates a step in the formation of an embodiment of the thin film transistor, namely the conversion of starting semiconductor

material into semi-amorphous semiconductor material through the application of a current. In Figure 6G, "current I flows through the regions 71, 72, and 74." Below is an annotated copy of Figure 6G:



The specification describes 71 and 72 as "impurity injected regions" and 73 and 74 as "non-impurity-injected regions."

In a January 8, 1997 rejection of the pending '463 patent claims, the examiner stated that "Matsumura teaches a thin film fet [field effect transistor] comprising . . . a channel layer with junctions to n-type amorphous silicon source and drain regions. . ." A full certified translation of Matsumura indicates that the reference discloses junctions that make ohmic contact between the drain and channel regions. However, the patent examiner

considered only a partial translation of the Matsumura reference. (It is unclear from the evidence submitted by the parties whether the partial translation included the reference's use of the term "ohmic contact.")

3. Dictionary and textbook definitions

"Junction" has been defined generally as:

- "a region of transition between two different semiconducting regions in a semiconductor device, such as a pn junction, or between a metal and a semiconductor," Dictionary of Scientific and Technical Terms 1076 (1994);
- "the transition boundary between semiconductor regions of different electrical properties (for example: N-N^+, P-N, P-P^+ semiconductors, or between a metal and a semiconductor)," IEEE Standard Dictionary of Electrical and Electronic Terms 563 (6th ed. 1996); and
- "a place where things join or meet" and "a layer or boundary which serves as the interface between semiconductor regions with different properties. For example, a *pn* junction. Also called semiconductor junction," Wiley Electrical and Electronics Engineering Dictionary 400 (2004).

"Junction, rectifying" is defined as "a region between two materials, typically N-type or P-type semiconductors, or between a metal and a semiconductor, arranged to provide a very low resistance to current flow in one direction and a very high resistance to current flow in the opposite direction." IEEE Standard Dictionary of Electrical and Electronic Terms 563.

Various references term N^+I contacts ohmic contacts. "Deposition of an n^+ a-Si:H layer between undoped a-Si:H and a metal allows the formation of an ohmic contact between them." Cherie R. Kagan and Paul Andry, Thin-Film Transistors 57 (2003). "In many cases a thin n+ a-Si:H layer is sandwiched between the metal electrode and the undoped a-Si:H to make ohmic contacts." Hideharu Matsuura et al., "Ohmic Contact Properties of Magnesium Evaporated Onto Undoped and P-Doped a-SI:H," Japanese Journal of Applied Physics, VOL. 22(3), L197-199 (Mar. 1983). "[G]ood ohmic contact was made because the i layer and the n^+ layer were sequentially deposited without breaking vacuum." H. Hayama and M. Matsumura, "a-SI FET IC Integrated on a Glass Substrate," National Convention Record, Institute of Electrical and Comm. Engineering of Japan 287-88 (Mar. 1980).

4. "Junction" as used in other patents

The '941 and '463 patents share the same specification and claim priority. During the prosecution of the '941 patent, plaintiff attempted to add the term "non-ohmic

junctions" to the pending claims. However, plaintiff withdrew those claims later, saying that there was an "absence of *explicit* support for this term [non-ohmic] in the specification." Dkt. #234, Exh. 102 at 15 (emphasis in original). The '941 patent has claims that recite the phrase "junctions in contact." Claim 15 of the '941 patent uses the phrase "junctions in contact" to refer to two interfaces and uses the term "ohmic contact" to refer to another interface:

> a channel region extending between said source and drain regions to form junctions in contact therewith . . .
>
> * * *
>
> an electrode in an ohmic contact with one of said source and drain regions.

In prosecuting its U.S. Patent Application No. 08/214,494 (the '494 application), plaintiff distinguished junctions from ohmic contacts. (The '494 patent application is not in the same family as the '463 patent.) Specifically, plaintiff distinguished U.S. Patent No. 4,766,477 (to Nakagawa), which discloses a transistor with ohmic contacts, explaining that:

> Moreover, to further distinguish over Nakagawa, all claims have been amended to recite that junctions are respectively formed between the source and drain regions and the intrinsic region of the horizontal IGFET of the claims whereas in Nakagawa ohmic contacts are made between source and drains 102 and 103 and channel layer 101.

All independent claims of the related '636 patent recite the limitation "source and drain regions forming respective junctions with said channel region." In SEL I, inventor

Yamazaki testified that junctions are "quite different" from ohmic contacts. He described an ohmic contact as having low resistance and linear characteristics. Yamazaki also stated that "you could have a PI, an NI or a PN junction but they have non-linear characteristics." Yamazaki Dep., Feb. 27, 1998, dkt. #210, Exh. 79 at 1386-1387 and 1389.

On February 26, 1998, plaintiff's expert in SEL I, Dr. Gerald Lucovsky, testified:

> Q. And does the source region in Fig. 1 make an ohmic contact to the channel region in this structure?
>
> A. The word ohmic contact is not an appropriate word to use for these contacts. These contacts are set up to be blocking under one set of applied potentials and to deliver and receive current under another set of those conditions. And in general, in order to make a transistor of this sort, that contact by definition is more akin to a semiconductor junction than an ohmic contact; that is, it delivers different amounts of current according to how it's driven electrically.

Lucovsky Dep., Feb. 26, 1998, dkt. #210, Exh. 78 at 121. In a later SEL I deposition taken on April 6, 1998, Lucovsky testified that:

> Q. Is the contact between the N plus source which is 107 and the amorphous silicon layer 105 which is intrinsic, an ohmic contact?
>
> A. That contact has added, as I said before and many, many times it has added a semiconductor junction. It has a semiconductor junction because inherently and intrinsically whenever you have, a region, two regions of different conductivity type in contact with one another, there is a semiconductor junction at that interface. The current flow out of the contact can have an ohmic character if the contact can supply as much current as the material calls for.

> So therefore, what I'm saying is that it would be an oversimplification and it would be an incorrect scientific statement to characterize that contact simply as ohmic because what you're doing is essentially clipping off, or if you would, taking a piece out of the context of the definition but not including the full understanding of it, and I want to make sure that we don't have any ambiguity where we don't understand what we're talking about and use words loosely.

Dkt. #292, Exh. 51 at 534-35. Later in that same deposition, Lucovsky made clear that junction and ohmic contacts are not mutually exclusive:

> Q. Have you had any tests done, or have you done any tests to determine whether the source to channel and drain to channel boundaries of any Samsung TFT are ohmic contacts?
>
> A. Let me say it again, the source to channel and drain to channel contacts are N plus I interfaces and as Dr. Fonash, Drs. Wronski, Nikkei and every textbook teaches, there are semiconductor junctions at those contacts. Under certain conditions of the applied current and voltage that are in the operating region of a thin film transistor, those carriers supply current as needed using the Al Rose definition. Therefore those junctions act as ohmic contacts, okay? And I prefer you say the word they act as ohmic contacts, not to have a bifurcation between the word ohmic contact on the one hand and the word semiconductor junction on the other. That's wrong. That's blatantly incorrect.

Id. at 547-48. Similarly, in a March 1998 declaration in that case, Lucovsky averred:

> Therefore, the '636 patent defines in a clear and unambiguous way the ni semiconductor junctions of the IGFET/TFT device structure. This definition is in complete agreement with the prevailing understanding of ni junctions as they are defined by Drs. D.E. Carlson, and C.R. Wronski in Exhibits 2 and 3, by Dr. Fonash on pages 89 and 90 of his deposition testimony. . . . They refer to these contacts as ohmic, which correctly describes the current flow at any particular value of gate bias voltage, but choose to ignore that there must be potential steps at the ni interface (i.e., a junction) in order for the IGFET/TFT structure to operate as a transistor device.

Lucovsky decl., Mar. 25, 1998, dkt. #292, Exh. 75, ¶ 17.

In a claim construction brief in SEL I, the defendants stated that "'junction,' as conventionally understood by those of skill in the art, includes 'ohmic contacts'" and agreed with Lucovsky's testimony that those of ordinary skill in the art consider "junctions" to encompass ohmic contacts. However, defendants argued that "Dr. Lucovsky's declaration is wrong as to the meaning of the term 'junction' in the Asserted Claims [of the '636 patent] because Dr. Yamazaki and SEL narrowed the meaning of that term during the prosecution history." Dkt. #289, Exh. 2 at 14. According to defendants, "[t]he prosecution history of the '636 patent reveals that, regardless of how the term junction is normally used, in the claims of the '636 patent 'junction' must be interpreted to exclude 'ohmic contacts.'" Id. at 12.

5. Accused products

A spectrometry analysis on an accused product shows that the NSI layer is a highly doped semiconductor material, which is referred to as a N^+-type material. Recipe files for many of the accused products show that the AH layer does not contain any N-type or P-type impurities. The NSI and AH layer in those products form an N^+I interface. At his deposition, defendants' engineer, Seok Je Seong, testified that "n^+ Si" is N^+ silicon, which is a material that "is used for the creation of ohmic contact" with the "source-drain." S.J.

Seong Dep. Vol. 2, dkt. #266 at 123. He also testified that "[o]hmic contact refers to a situation where as the pressure—correction—as the voltage is increased, commensurate with that, the current is increased as well." S.J. Seong Dep. Vol. 1, dkt. #265 at 39-40.

F. "Non-Single Crystal Semiconductor"

1. Intrinsic evidence

Claims 1, 5, 12 and 13 recite source and drain regions comprising a "non-single crystal semiconductor material." The '463 patent specification says:

> The non-single crystal semiconductor 7 means a semi-amorphous semiconductor, an amorphous semiconductor or a mixture thereof and it is desired to be the semi-amorphous semiconductor. The semi-amorphous semiconductor is formed of a mixture of microcrystalline semiconductor and a non-crystalline semiconductor and the mixture is doped with a dangling bond neutralizer and the microcrystalline semiconductor has a lattice strain.

Col. 3, lns. 37-39.

> In the case where the non-single crystal semiconductor 7 is formed of the semi-amorphous semiconductor (which will hereinafter be referred to as a starting semi-amorphous semi-conductor), the region Z2 is transformed by the heat generated by the current I into the semi-amorphous semiconductor S2 which contains the microcrystalline semiconductor more richly than does the starting semi-amorphous semiconductor. Even if the non-single crystal semiconductor 7 is the amorphous semi-conductor or the mixture of the semi-amorphous and the amorphous semiconductor, the semi-amorphous semiconductor S2 is formed to have the same construction as in the case where the non-single crystal semiconductor 7 is the semi-amorphous one.

Col. 8, lns. 18-30.

The specification discusses the relative stability of the semi-amorphous semiconductor and the non-single crystal semiconductor, stating that "the semi-amorphous semiconductor S2 has stable properties as semiconductor, compared with the non-single crystal semiconductor 7." Col. 8, lns. 64-67. It also says that the "semi-amorphous semiconductor S2 assumes stable states as compared with . . . the amorphous semiconductor . . . ." Col. 9, lns. 48-50.

The specification explains that the semi-amorphous material provides "excellent properties" as a semiconductor device, col. 9, lns. 56-67, and adds that

> The non-single crystal region S1 does not possess the above said excellent properties of the semi-amorphous semiconductor region S2. Especially, the region S1 does not have the excellent conductivity characteristic of the region S2 and the former can be regarded as an insulating region relative to the latter. Consequently, the non-single crystal semiconductor region S1 electrically isolates the semi-amorphous semiconductor regions S2 from adjacent ones of them.

Col. 9, lns. 62-67; Col. 10, lns. 1-3. The specification explains that to manufacture source, drain and channel regions, amorphous semiconductor material is heated and "undergoe[s] a structural change into semi-amorphous semiconductor" material, which makes up the source, drain, and channel regions:

> Next, a description will be given, with reference to FIGS. 6A to 6H, of a second embodiment of the semiconductor device of the present invention, together with its manufacturing method.

* * *

> . . . the regions 71, 72 and 74 respectively undergo a structural change into semi-amorphous semiconductor regions 77, 78 and 79, respectively, as shown in FIG. 6H.
>
> In this way, the semiconductor device of the second embodiment of the present invention is obtained.

Col. 10, lns. 34-37 and col. 11, lns. 18-29.

> In the semiconductor device of the present invention shown in FIG. 6H, the regions 77, 78 and 79 correspond to the semi-amorphous semiconductor region S2 in FIG. 1G, providing excellent properties as a semiconductor device. The region 73 corresponds to the non-single crystal semi-conductor S1 in FIG. 1G, and hence it has the property of an insulator. The regions 77, 78 and 79 are encompassed by the region 73, so that the regions 77 to 79 are essentially isolated from the other adjoining regions 77 to 79 electrically.

Col. 11, lns. 30-38.

> Moreover, the semi-amorphous semiconductor forming the semiconductor device of the present invention permits direct transition of electrons even at lower temperatures than does the amorphous semiconductor.

Col. 12, lns. 62-65.

2. Extrinsic evidence

One textbook states that "[s]ingle-crystal materials have more uniform and predictable properties than polycrystalline materials." Peter Van Zant, Microchip Fabrication 51 (3d ed. 1997).

In a June 9, 2003 claim construction order in Acer, Judge Alsup determined that "non-single crystal semiconductor material" as used in the '941 patent should be construed as it is defined in the specification, which is the same specification used in the '463 patent.

Regardless whether an amorphous or semi-amorphous semiconductor is used, using silicon nitride instead of silicon oxide in the gate insulator provides a thin film transistor with better resistance to degradation while still insulating the channel region from the gate electrode of the thin film transistor.

G. "Intrinsic" Amorphous Semiconductor Material

Claims 5 and 13 state that the channel region comprises "an intrinsic amorphous silicon semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof." These claims also recite "said pair of source and drain regions . . . having a P or N type conductivity to form PI or NI junctions in contact with said channel region."

The '941 patent also recites the claim limitation of an "intrinsic" semiconductor material. On February 27, 1998, Yamazaki testified as follows with respect to the '941 patent at issue in SEL I:

> Q. Then it goes on to say "We should seek Dr. Yamazaki's further comments on the particular advantages of the intrinsic semiconductor in this

> context for use in the interview presentation." Dr. Yamazaki, my question to you is are there other advantages that you're aware of?
>
> A. The general meaning of I type is one in which there are as few impurities as possible. Therefore, if you put in P or N type impurities deliberately, or if oxygen which results in N type characteristic gets in, then the characteristics deteriorate.

Dkt. #210, Exh. 79 at 1448. In Acer, plaintiff's proposed construction of "intrinsic" was "not intentionally doped with an efficient dopant." However, the court found that the proposed construction invited "controversy as to what counts as an efficient dopant." In the final claim construction order, Judge Aslup wrote:

> **At this juncture, this order holds that "intrinsic" refers to pure or near pure semiconductor material that has not previously been doped.** . . .
>
> To the extent any further construction is required, it will await additional expert testimony regarding the meaning of intrinsic as applied to amorphous or semi-amorphous semiconductor materials.

Dkt. #290, Exh. 288 at 7 (emphasis in original). The '463 patent cites the final claim construction order in Acer as a reference.

H. Sakamoto Reference

Japanese Patent Publication No. 55-19820 ("Sakamoto"), entitled "Semiconductor Device," was filed on July 27, 1978 and published on February 12, 1980, before the '463 patent's claimed priority date of June 30, 1980. However, plaintiff did not provide the

Sakamoto publication to the U.S. Patent and Trade Office during the prosecution of the '463 patent. Sakamoto discloses semiconductor devices that may be used in integrated circuit memory.

Sakamoto teaches two embodiments of a thin film transistor. The second embodiment is depicted in Figure 2 below. (The regions marked 202, 203, 204 and 205 have been shaded and labeled by defendants in this version of Figure 2.)

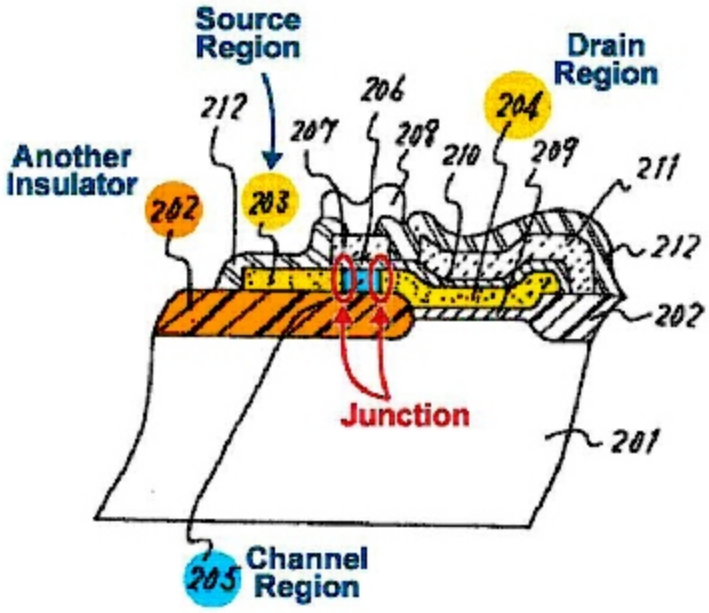


Fig. 2

The second embodiment of Sakamoto discloses all of the elements of the asserted '463 patent claims except for (1) an amorphous source, drain and channel region doped with a "recombination center neutralizer, such as hydrogen, a halogen, or a combination thereof" and (2) an "intrinsic channel region." Although Sakamoto states that the source and drain regions contain "effective dopants," it does not define that term. Figure 2 shows dots in the

source and drain regions, labeled as 203 and 204, without any explanation of the meaning of the dots. The channel region in Figure 2 does not contain any dots.

In the second embodiment, Sakamoto also sets forth the following steps for constructing a Metal Oxide Semiconductor (MOS) field-effect transistor, which is a thin film transistor:

> In the MOS field-effect transistor for the cell unit, either the first polysilicon or amorphous silicon film 203 or 204 that is formed on the thick silicon oxide film containing effective dopants is used as a source or drain, respectively; and similarly, a part of the surface of the either polysilicon or amorphous silicon film 205 is used as a channel region; and the thin insulator 206 (for example, a silicon nitride film), the second polysilicon or amorphous silicon film 207 containing dopants, and the metallic electrode 208 are used as the gate film, the gate electrode, and the word line in the MOS field-effect transistor, respectively.

Dkt. #208, Exh. 6 at 3. Sakamoto explains that the channel is formed in "a part of the surface of . . . amorphous silicon film 205." Id. The amorphous silicon thin film transistor that Sakamoto discloses has source and drain regions doped with N-type or P-type impurities.

I. Amorphous Silicon and Recombination Centers

Amorphous silicon is cheaper to fabricate than single crystal or polycrystalline silicon. It can be made at low temperatures, allowing the use of "cheaper" material (such as glass substrates instead of quartz or silicon) on which to build devices. Amorphous silicon can be

formed by the processes of evaporation or sputtering. However, as explained in plaintiff's Japanese Patent Application No. 55-88974 (JP '974), to which the '463 patent claims priority:

> Because it is random in all aspects, the amorphous semiconductor is not necessarily stable in terms of free energy as compared with crystalline semiconductor . . . and, owing to its random property, there exist in the amorphous semiconductor a large number of dangling bonds which are no[t] chemically bonded with each other. The dangling bonds serve as recombination centers which extremely reduce the carrier life.

The parties agree that, in other words, dangling bonds in amorphous silicon act as recombination centers that can trap charged particles (charge "carriers").

Amorphous silicon formed by evaporation or sputtering does not include a recombination center neutralizer unless one is added by a process called doping. When Sakamoto was filed in 1978, it was known that dangling bonds in amorphous silicon could be neutralized by doping the material with hydrogen or a halogen. (Halogen refers to a group of highly reactive elements including fluorine, chlorine, bromine, iodine and astatine.) Amorphous silicon doped with hydrogen (a-Si:H) as a recombination center neutralizer is referred to as "hydrogenated amorphous silicon."

According to R.A. Street, Hydrogenated Amorphous Silicon 1 (Cambridge University Press 1991), hydrogenated silicon was first made in the late 1960s. Before that time, research on amorphous silicon without hydrogen showed that it has a "very high defect

density, which prevents doping, photoconductivity and other desirable characteristics of a useful semiconductor." Id. Street explains that it was discovered later that amorphous silicon could be made from silane gas (SiH_4) by a technique called glow discharge:

> The essential role of the hydrogen in a-Si:H was first recognized . . . at Harvard . . . . They understood that the high defect density of amorphous silicon . . . prevented [it] from being useful for electronic devices and tried to find ways of eliminating the defects, eventually succeeding by introducing hydrogen into the sputtering system. The hydrogen caused a similar improvement in the material properties as was found for glow discharge a-Si:H, with a high photoconductivity, low defect density and doping. . . . Shortly after the Harvard experiments, it was confirmed that the glow discharge material also contained hydrogen. . . . This is now recognized as an essential component of the films which is responsible for suppressing defects.

Id. at 2. "A major turning point in the development of a-Si:H was the report in 1975 of substitutional n-type or p-type doping by the addition of phosphine or diborane to the deposition gas (Spear and LeComber 1975)." Id. SiH_4 has "good electrical transport properties with a fairly high carrier mobility . . . and also strong photoconductivity resulting from a very low defect density . . . ." Id. at 1.

Using hydrogen or a halogen as a recombination center neutralizer was known and accepted by at least some academics prior to the alleged invention of the '463 patent. By the time the '463 patent was filed (priority date of June 30, 1980), glow discharge decomposition of silane was a known technique in the art. Also at this time, it was known that amorphous silicon could be deposited through a technique known as glow discharge

decomposition of silicon tetrafluoride (SiF_4) to produce amorphous silicon doped with fluorine (a halogen). Doping amorphous silicon with hydrogen as a dangling bond neutralizer is admitted prior art in the '463 patent file history.

Transistors constructed from pure amorphous silicon are less effective than those constructed from doped amorphous silicon. Silicon has an important advantage over other semiconductor materials because its conductivity can be improved by the addition of N-type or P-type impurities. Doping amorphous silicon with N-type or P-type impurities allows the source and drain regions to form in a single layer of amorphous silicon semiconductor material. U.S. Patent No. 4,217,374 (Ovshinsky '374), which was filed on March 8, 1978, states:

> Accordingly, a considerable effort has been made to develop processes for readily depositing amorphous semiconductor films, each of which can encompass relatively large areas, if desired, limited only by the size of the deposition equipment, and which could be readily doped to form p and n junctions where p-n junction devices are to be made therefrom equivalent to those produced by their crystalline counterparts. For many years such work was substantially unproductive. Amorphous silicon or germanium (Group IV) films were found to have microvoids and dangling bonds and other defects which produce a high density of localized states in the energy gap thereof. The presence of a high density of localized states in the energy gap of amorphous silicon semiconductor films results in a low degree of photoconductivity and short diffusion lengths, making such films unsuitable for solar cell applications. Additionally, such films cannot be successfully doped or otherwise modified to shift the Fermi level close to the conduction or valence bands, making them unsuitable for making p-n junctions for solar cell and current control device applications.

U.S. Patent No. 4,226,898 (Ovshinsky '898), which was filed on March 16, 1978, contains a similar statement.

J. "Recombination Center Neutralizers" in other Prior Art

Before the June 1980 priority date of the '463 patent, a number of publications disclosed the use of *hydrogen* as a recombination center neutralizer in amorphous silicon: W.E. Spear and P.G. LeComber, "Investigation of the Localised State Distribution In Amorphous Si Films," Journal of Non-Crystalline Solids (1972); A. Madan, Electronic Transport and State Distributions in Amorphous Silicon Films 29 (1973); M. Hirose et al., "Electronic Density of States in Discharge-produced Amorphous Silicon," Applied Physics Letters 34:3, p. 1 (1979); H. Hayama and M. Matsumura, Amorphous Silicon Thin-Film MOS Transistors, Transactions of the Institute of Electrical and Communication Engineering of Japan J63-2 (Feb. 1980); and H. Hayama, "Amorphous Silicon Thin-film Metal-Oxide-Semiconductor Transistors," Applied Physics Letters (May 1980).

Before June 1980, the following publications disclosed the use of *either a halogen or hydrogen* as a recombination center neutralizer in amorphous silicon: JP '974; U.S. Patent No. 4,217,374 (Ovshinsky '374) (filed Mar. 8, 1978); W.E. Spear, "Introductory Talk: Localized States In Amorphous Semiconductors," Proc. Fifth International Conference on Amorphous and Liquid Semiconductors 6 (1974); A. Madan et al., "Investigation of the

Density of Localized States in a-Si using the Field Effect Technique," Journal of Non-Crystalline Solids 20, 239-57 (1975); A.K. Malhotra and G.W. Neudeck, "Effects of Hydrogen Contamination on the Localized States in Amorphous Silicon," Applied Physics (1976); and P.G. Le Comber et al., "Amorphous-silicon Field-effect Device and Possible Application," Electronics Letters (1979). (The parties dispute whether the following references disclose the use of hydrogen or a halogen as a recombination center neutralizer for amorphous silicon: U.S. Patent No. 4,226,898 (Ovshinsky '898) (filed Mar. 16, 1978); JP 55-50663 (published Apr. 12, 1980); and JP 55-50664 (published Apr. 12, 1980); H. Hayama and M. Matsumura, "a-Si FET IC Integrated On A Glass Substrate," National Convention Record, Institute of Electrical and Communication Engineering of Japan 287-88 (Mar. 1980)).

(Although plaintiff cites several references that allegedly disclose thin film transistors composed of amorphous silicon without a recombination center neutralizer, it has not proposed a finding of fact to that effect. Instead, it cites the references only in its briefs or in response to defendants' proposed findings of fact. Therefore, I have not considered those references.)

During prosecution of the '463 patent, the examiner rejected the pending claims in light of U.S. Patent No. 4,485,389 (Ovshinsky '389), which identifies "current control

devices" as including "transistors" and explains that fluorine can be used as a recombination center neutralizer. Also during prosecution of the '463 patent, plaintiff stated in 1991 that

> Typically with amorphous semiconductor materials, the dangling bond neutralizer doping level may be as high as 25 to 30 mol% in order to insure termination of all of the dangling bonds present in such amorphous material. However, due to the presence of crystalline structures in semi-amorphous semiconductor material, there are less dangling bonds and therefore less dangling bond neutralizer can be utilized to terminate the dangling bonds.

Dkt. #303, Exh. 508 at 4-5. Later, during the '463 patent prosecution in 1994, plaintiff stated that

> [A]lthough hydrogen as a dangling bond neutralizer in general for amorphous materials, for example, was known as evidenced by column 3 of Ovshinsky's discussion of the prior art, the fact remains that there is no recognition or suggestion whatsoever in Oshinsky to use hydrogen alone in the 1-5% range.
>
> Applicant acknowledges that hydrogen alone was known as a dangling bond neutralizer for amorphous semiconductor materials. In fact, as discussed at column 6, lines 49-68 of U.S. Patent 4,409,134, of record, to the applicant S. Yamazaki, 20-30% of hydrogen is necessary to terminate the numerous dangling bonds that exist in amorphous semiconductor material. However, with the SAS material of the present invention, there are less dangling bonds to be terminated and thus hydrogen alone can be used in an amount less than 5 mol%, as recognized by the applicant S. Yamazaki, for SAS material.

Dkt. #208, Exh. 14 at 7.

K. Matsumura Reference

In March 1980, Drs. Hiroshi Hayama and Masakiyo Matsumura of the Tokyo Institute of Technology published a paper titled "a-Si FET IC Integrated on a Glass Substrate" (Matsumura). (The reference is prior art to the '463 patent and was cited by the patent examiner during the '463 patent prosecution.) Matsumura discloses an amorphous silicon thin film transistor with all the elements of the asserted '463 patent claims except a silicon nitride gate insulating film.

L. LeComber

P.G. LeComber, "Amorphous Silicon Field Effect Device and Possible Applications," Electronics Letters, V. 15, No. 6 (Mar. 15, 1979) is prior art to the '463 patent and was considered by the patent office during the prosecution of the '463 patent. Like Matsumura, LeComber focuses on amorphous silicon thin film transistors. LeComber discloses a thin film transistor designed for use in an LCD panel, specifically an insulated-gate field-effect transistor made of amorphous silicon deposited by a glow discharge technique. One embodiment disclosed in the reference shows two thin film transistors with source, drain and gate electrodes. The channel region disclosed in LeComber consists of amorphous silicon and the gate insulator consists of silicon nitride.

M. Gate Insulators

Although the composition of the gate insulators disclosed in Matsumura (silicon oxide) and LeComber (silicon nitride) differ, both types of gate insulators serve the same function of insulating the gate electrode from the channel region, which allows the transistors to switch on and off. Matsumura and LeComber were well known to those of ordinary skill in the art in the late 1970s. Further, a person of ordinary skill in the art likely would have known that Matsumura had cited the work of LeComber in certain papers. For example, Matsumura and Hayama published an article entitled "Amorphous-Silicon Thin-Film Metal-Oxide-Semiconductor Transistors" in Applied Physics Letters, Vol. 26, No. 9, on May 1, 1980, in which they cited LeComber on gate insulators.

At the time of the alleged invention of the '463 patent (June 1980), it was well known that a crystalline transistor with silicon nitride provided better protection against harmful charged particles than one with silicon oxide and was more resistant to radiation exposure. Following the filing of the '463 patent, people of skill in the art continued to analyze the use of silicon nitride insulators in amorphous silicon thin film transistors. For example, an article published by M.J. Powell in 1985 compared silicon oxide and silicon nitride gate insulators and noted advantages and disadvantages to both. A 1989 paper by Powell described further investigations of the differences between these insulators and concluded that nitride is superior to oxide in amorphous thin film transistors.

N. Matsumura and LeComber in SEL I

In SEL I, plaintiff brought claims that defendants' LCD products infringed U.S. Patent 5,543,636 (the '636 patent). The U.S. District Court for the Eastern District of Virginia found the '636 patent unenforceable for inequitable conduct in part because plaintiff disclosed to the patent office only a partial translation of Japanese Application No. 56-135968 (Canon), which discloses the combination of an amorphous silicon thin film transistor with a silicon nitride gate insulator.

In a subsequent motion for reconsideration, plaintiff argued that the court erred in finding that Canon was not cumulative of other information before the patent office, including Matsumura and LeComber. In support of its argument, plaintiff filed a declaration by Dr. Masakiyo Matsumura, who averred that Figure 1 in his reference shows, among other things, an undoped or intrinsic amorphous silicon semiconductor layer, an n^+ or doped source and drain with aluminum electrodes and a silicon oxide (SiO_2) gate insulator. He averred that the channel region is formed in the undoped or intrinsic amorphous silicon semiconductor layer between the n^+ source and drain. Matsumura also averred that the amorphous silicon of the source, drain and channel regions was deposited by "glow discharge" or the decomposition of silane.

Also in support of its motion for reconsideration of the inequitable conduct ruling, plaintiff submitted a claim chart showing that the following claim limitations in the '636

patent were disclosed by Matsumura: (a) a "TFT" or thin film transistor; (b) "Intrinsic Amorphous Silicon Semiconductor layer with [a] Channel Region;" and (c) a channel region "Sandwiched between [a] Gate Insulator and Another Insulator." The chart also shows that as compared to Canon, Matsumura is missing the limitations of a "Silicon nitride gate Insulator" and the concentration limits on carbon (C), nitrogen (N) and oxygen (O) in the channel region. Plaintiff admitted in its motion for reconsideration that Matsumura disclosed the co-planar thin film transistor structure from the '636 patent with the exception of its silicon nitride gate insulator:

> Fig. 1 [of Matsumura] . . . discloses a coplanar TFT with the same intrinsic amorphous silicon sandwiching structure found in the '636 patent. The only difference in structure is the gate insulator. In Matsumura, the gate insulator is made of silicon oxide rather than silicon nitride.

In his declaration, Dr. Matsumura averred that he knew from a paper by P.G. LeComber, entitled "Amorphous Silicon Field Effect Device and Possible Applications," that silicon oxide can be replaced by silicon nitride as the gate insulator.

> In its motion for reconsideration, plaintiff stated the following:
>
> The combination of silicon nitride with the intrinsic amorphous silicon sandwiching structure in Matsumura, however, is suggested by other information before the [US]PTO.
>
> * * *
>
> [I]n a . . . Information Disclosure Statement filed with the Patent Office . . ., the use of silicon nitride as a gate insulator was spelled out from [sic] the

Examiner several times, including in connection with the discussion of Matsumura's intrinsic amorphous silicon sandwich structure. The pertinent portions from . . . the IDS state the following:

> [T]he following Japanese Patents disclose the use of silicon nitride for a gate insulating layer of a thin film transistor: 56-135968, 55-50663 and 55-50664.
>
> * * *
>
> The Examiner's attention is particularly directed to Reference (18) to LeComber et al. which appears to disclose the use of a silicon nitride layer as a gate insulator.
>
> * * *
>
> Reference (12) to Matsumura teaches a TFT having a non-doped i-type amorphous silicon film formed on a glass substrate, n+ layers as source and drain regions formed on the i-type silicon film and a silicon oxide (SiO_2) layer as a gate insulating layer.

Thus, having a single reference showing silicon nitride in combination with the intrinsic amorphous silicon sandwiching structure is not material, given that the combination is clearly taught by other information before the PTO. As noted above, this other information informed the Examiner of the prior art use of silicon nitride as a gate insulator and its known interchangeability with silicon oxide.

Dkt. #209, Exh. 35 at 12-13.

O. Matsumura and LeComber in the '463 Patent Prosecution

During the prosecution of the '463 patent, the examiner rejected the application several times before issuing a final rejection of the claims as obvious over Matsumura in view of LeComber, Yamazaki '330, Ovshinski '941, Madan, and Yamazaki '663. (Although the parties do not say so, I assume that the "Yamazaki" named in these references refers to the named inventor on the '463 patent.) Plaintiff appealed the examiner's final rejection to the Board of Patent Appeals and Interferences, arguing that it would not be obvious to combine Matsumura and LeComber because they disclosed different types of transistors:

> Also, with respect to LeComber, it is important to note that the type of transistor disclosed by LeComber is entirely different from the transistor disclosed by Matsumura. That is, while the transistor disclosed by Matsumura has junctions between two semiconductor materials having different conductivity type, the transistor of LeComber utilizes Schottky junction, that is, a semiconductor-oxide-metal junction. As noted above, unique problems (that are clearly not disclosed or suggested by the prior at [sic]) result in a device having such junctions, which are not present in the device of LeComber.

In a November 30, 1999 answer to the appeal, the patent examiner explained that using halogen to reduce dangling bonds in amorphous semiconductor material was "fundamentally obvious from the teachings of Yamazaki '330 and Ovshinsky '941." Dkt. #224, Exh. 264 at 4-5. "Both Yamazaki and Ovshinsky recognized the advantages of including hydrogen or halogen . . . in amorphous semiconductor material to improve device function." Id. The examiner also noted that nitride had been disclosed as a gate insulating film in the prior art and stated that

> Both silicon oxide and silicon nitride gate insulating films in field effect transistor devices were well known at the time of applicant's invention and there is clearly a preponderance of evidence that their practice in thin film transistor devices was not and would not have been unobvious.

Id. at 5-6.

On May 27, 2004, the Board of Patent Appeals and Interferences allowed the claims of the '463 patent to issue over the considered references. In reversing the patent examiner's rejection, the board noted that the examiner relied on LeComber and Madan for a gate insulating film comprising a nitride and on Matsumura for the general teaching related to the claimed source, drain and channel regions, even though Matsumura does not teach silicon oxide gate insulating films. It found that the examiner had not "provided a convincing rationale as to why Le Comber, taken with Matsumura, would have rendered obvious the proposed modifications." Dkt. #224, Exh. 265 at 5. The board determined that "LeComber would not have been considered by the artisan as applicable to the type of device disclosed by Matsumura, and thus would not have suggested modification of the device. . . [T]he references disclose different structures, and LeComber does not discuss the reference's teachings as applied to other environments." Id. The board found "no suggestion that the silicon nitride film used in the IGFET [i.e., "insulated gate field effect transistor"] is also recommended, or even suitable, for a device having the type of junctions in the Matsumura device." Id.

P. Kazmerski Reference

Polycrystalline and Amorphous Thin Films and Devices is a book edited and published by Lawrence L. Kazmerski in 1980 as part of the "Materials Science Series." Chapter 6 of the book is entitled "Amorphous Thin-Film Devices" and section 6.4.6 is entitled "Thin-Film Transistors." Figure 6.16 of this reference depicts a silicon oxide gate insulating film (labeled "OXIDE") arranged between a gate electrode and an a-Si:H film:

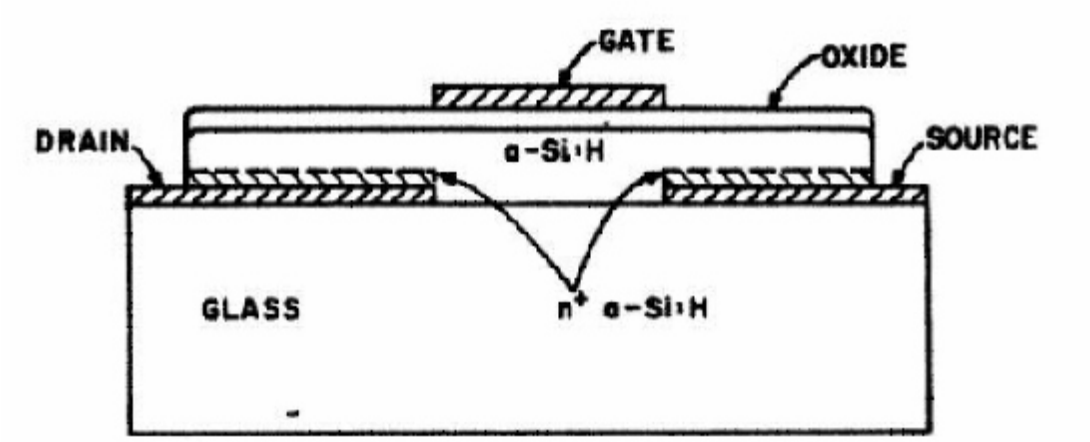


Fig. 6.16 Schematic drawing of an a-Si:H MOS TFT.

On the same page that Figure 6.16 appears in the reference, Kazmerski states:

> Spear and LeComber [75] used a similar field-effect type of device to determine the density of states in a-Si:H. However, in that early work, a glass substrate (~250 *J-tm* thick) was used as the insulating layer between the gate electrode and the a-Si:H. Thus gate voltages as large as 1 kV had to be applied to modulate the drain current by a factor of 10^3. In later work by Madan et al. [46] a thin film of amorphous Si_3N_4 (~1-3 *J-tm* thick) was used as the

> insulating layer, and then gate voltages of ~ 50 V were able to produce a modulation of ~ 10^3 in the drain current.
>
> More recently, L. A. Goodman [76] at RCA Laboratories has succeeded in fabricating a-Si:H TFTs using a metal-oxide semiconductor (MOS) structure (see Fig. 6.16). The source and drain contacts were made by depositing a thin layer (~300 A) of phosphorus-doped a-Si:H on top of· a Cr film on glass and then using photolithography to define the electrode pattern. The spacing between the source and drain was 10 *J-tm*, and the channel width was 320 *J-tm*. The undoped a-Si:H was usually deposited to a thickness in the range of 0.1-0.5 *J-tm*. The Si02 layer was typically 0.1-0.2 *J-tm* thick and was deposited either by electron-beam evaporation or by sputter deposition. The Cr gate electrode was also defined using photolithography.

Dkt. #289, Exh. 11 at 202. In other words, Kasmerski cited Madan (which was before the board during the prosecution of the '463 patent) for its teaching of silicon nitride as a gate insulator but explains that "more recently," a-Si:H thin film transistors have been fabricated using a metal-oxide semiconductor (MOS) structure. Later in the reference, Kazmerski explains that "[a]ll the a-Si:H devices we have discussed are still in the experimental stage" and "[a]morphous semiconductor TFTs may eventually find applications in large-area displays or flat -panel televisions." Id. at 204-05. He also noted that:

> The present challenge for scientists working in the area of amorphous semiconductors is to attain a better understanding of these materials so the experimental devices discussed in this article will become a practical reality. Moreover an improved understanding of amorphous semiconductors should allow new devices and applications to be developed in the future.

Id. at 205.

Q. JP '663 and '664

Japanese Patent Applications No. 55-50663 (JP '663) and No. 55-50664 (JP '664) were filed on October 7, 1978 and were published on April 12, 1980. They have almost identical specifications. The "Detailed Description of the Invention" section of the specification reads as follows:

> The present invention relates to the so-called a non-monocrystalline semiconductor, wherein at least a part of the channel region below the gate insulation substance of the insulated gate electric field transistor (hereinafter referred to as MIS-FET) is amorphous or polycrystalline; and wherein an inert gas, such as hydrogen, helium or neon, or a halide such as chlorine, is mixed in 0.1 mole % or greater; an objective being to neutralize and eliminate the recombination centers due to dangling bonds in this non-monocrystalline region.
>
> * * *
>
> The present invention makes it possible to sufficiently minimize the concentration of recombination centers, which is the fundamental cause of these problems, in a nonmonocrystalline (polycrystalline or amorphous) material, which is not monocrystal, and as a result, it has been completed for the first time.

The specification of both applications then provides an "explanation of the present invention based on an embodiment thereof" and sets out two different embodiments. Following the description of both embodiments, the specification states that

> It goes without saying that according to description explaining FIG. 1 and (A) and (B), wherein after devices are completed or mostly completed with "inductive curing" of such devices, one can remove not only the recombination centers in a single-crystal semiconductor, but also neutralization can be carried

> out with an inert gas such as [illegible], or hydrogen can be used as an inert gas on the interface level present on the interface between a polycrystalline or amorphous semiconductor and an insulation substance or a semiconductor and an insulation substance.

Figure 1(A) of both applications discloses a thin film transistor structure.

Claim 1 of JP '663 recites

> Semiconductor elements, wherein at least one part of the channel region of an insulated gate type field effect transistor is formed with a non-monocrystalline semiconductor, and an inert gas such as hydrogen, helium or neon, or a halogen compound such as chlorine, is mixed in said semiconductor with a concentration of at least 0.1 mole %.

Claim 1 of JP '664 recites

> Semiconductor elements, wherein second insulation gate-type field-electric transistors are provided, wherein at least a part of the source, drain, or channel region is formed with a nonmonocrystalline semiconductor, above the first gate-type field-electric transistors that are provided on a semiconductor substrate.

DISCUSSION

I. INFRINGEMENT ANALYSIS

A. Relevant Law

"'Summary judgment on the issue of infringement is proper when no reasonable jury could find that every limitation recited in a properly construed claim either is or is not found in the accused device either literally or under the doctrine of equivalents.'" U.S. Philips Corp. v. Iwasaki Electric Company, 505 F.3d 1371, 1374-1375 (Fed. Cir. 2007) (quoting PC Connector Solutions LLC v. SmartDisk Corp., 406 F.3d 1359, 1364 (Fed. Cir. 2005)). Patent infringement analysis involves two steps. First, the patent claims must be interpreted or construed to determine their meaning and scope. Markman v. Westview Instruments, Inc., 52 F.3d 967, 976 (Fed. Cir. 1995). Second, the properly construed claims are compared to the process or device accused of infringing. Id.

When construing claims, the starting point is the so-called intrinsic evidence: the claims themselves, the patent specification and the prosecution history. Teleflex, Inc. v. Ficosa North America Corp., 299 F.3d 1313, 1325 (Fed. Cir. 2002). Examination of the claims' language is the starting point for the well established process of claim construction. "Claim construction must adhere carefully to the precise language of the claims that the patent [examiner] has allowed." Ardisam, Inc. v. Ameristep, Inc., 336 F. Supp. 2d 867, 879 (W.D. Wis. 2004) (citing Autogiro Co. of America v. U.S., 384 F.2d 391, 396 (Ct. Cl.

1967)). The language is given its ordinary meaning as it would be understood by one of ordinary skill in the relevant art, given its context and the other patent claims. Rexnord Corp. v. Laitram Corp., 274 F.3d 1336, 1342 (Fed. Cir. 2001). However, "[t]he patent applicant may not have used words consistent with the dictionary definition because an applicant can act as his or her own lexicographer or may disavow or disclaim aspects of a definition 'by using words or expression of manifest exclusion or restriction, representing a clear disavowal of claim scope.'" Ardisam, 336 F. Supp. 2d at 879-80 (quoting Golight, Inc. v. Wal-Mart Stores, Inc., 355 F.3d 1327, 1331 (Fed. Cir. 2004)).

This initial construction must be considered in light of the specification to determine whether the inventor expressed a different meaning for the language, whether the preferred embodiment is consistent with the initial interpretation and whether the inventor specifically disclaimed certain subject matter. Rexnord, 274 F.3d at 1342-43. Finally, the interpretation is examined for consistency with the patent's prosecution history and any disclaimers made therein. Id. at 1343.

If necessary, a court may consult extrinsic evidence, such as dictionaries, treatises and expert testimony for background information and to "shed useful light on relevant art." Phillips v. AWH Corporation, 415 F.3d 1303, 1317 (Fed. Cir. 2005) (internal citations omitted). In general this type of evidence is less reliable than intrinsic evidence in determining the meaning of claim terms and is "unlikely to result in a reliable interpretation

of patent claim scope unless considered in the context of the intrinsic evidence." Id. at 1318-19.

Once the claims are properly construed, the plaintiff must prove that each claim element is present in the accused product, either literally or by equivalence, to establish infringement. Dawn Equipment Co. v. Kentucky Farms Inc., 140 F.3d 1009, 1015 (Fed. Cir. 1998). "Direct infringement requires a party to perform or use each and every step or element of a claimed method or product." BMC Resources, Inc. v. Paymentech, L.P., 498 F.3d 1373, 1378 (Fed. Cir. 2007). Plaintiff must prove infringement by a preponderance of the evidence. Nutrinova Nutrition Specialties and Food Ingredients GmbH v. International Trade Commission, 224 F.3d 1356, 1359 (Fed. Cir. 2000). Conversely, defendant can prevail by demonstrating that at least one element of the asserted claim is absent from its devices. Although in defending defendants' motion for summary judgment plaintiff need provide only enough evidence for a reasonable jury to find infringement of the claims and elements challenged by defendant, "a patentee who fails to provide probative evidence of infringement runs the risk of being peremptorily nonsuited." Novartis Corp. v. Ben Venue Laboratories, Inc., 271 F.3d 1043, 1050-51 (Fed. Cir. 2001). General or conclusory assertions are insufficient. TechSearch, L.L.C. v. Intel Corp., 286 F.3d 1360, 1372 (Fed. Cir. 2002).

B. Location of Channel Region

Underlying the question of infringement of all of the asserted claims is the meaning of "channel region" and its location with respect to the source and drain regions. The parties also dispute the composition and function of the accused products. As an initial matter, I note that plaintiff argues in response to some of defendants' proposed findings of fact that Dr. Fair (defendants' expert) did not make clear whether some of his opinions applied to all of the accused products. However, the parties did not raise this issue in their summary judgment briefs and defendants have not asserted that the evidence adduced by plaintiff does not apply generally to the accused products. In sum, the parties appear to agree that all of the accused products should be analyzed similarly with respect to infringement of the '463 patent.

On the question of non-infringement, defendants contend the following:

- The accused products do not infringe claims 1-7 and 12-13 because the source and drain regions in the accused products are not "in contact with the channel region."

- The accused products do not infringe any of the asserted claims because they do not have source and drain regions forming "junctions" (or non-ohmic contacts) with the "channel region."

- The accused products do not infringe claims 1, 5, 12 and 13 because the accused channel region is located below the source and drain regions, not "between" them.

- The accused products do not infringe claims 8, 9 or 14 because the accused source and drain regions are not located in one "semiconductor film" as the channel region, but rather in different layers.

At the center of the parties' dispute is the meaning of the terms "channel region," "between," "semiconductor film" and "junction."

1. Construction of "channel region"

Resolution of the meaning of this claim term requires a determination of what area the channel region encompasses in the claimed thin film transistor. Plaintiff asks the court to construe the term to mean "an area—labeled 79 in figure 6H of the '463 patent—between the source and drain regions through which the current path between the source and drain electrodes is formed; the channel region includes but is not limited to the current path between the source and drain electrodes." In other words, plaintiff would have the court define the channel region as including the entire area of semiconductor material between the source and drain regions. It bases its proposed construction in part on the court's construction of the term in Acer, addressing the '941 patent, which has the same specification as the '463 patent. Defendants do not propose a specific definition for the term channel region and instead focus on identifying where the channel region would be located in the accused products.

A few initial matters deserve mention. Plaintiff's proposed construction includes a definition of channel agreed to by the parties in Acer, namely "the current path between the source and drain electrodes." Although defendants challenge the construction in their reply brief, dkt. #321 at 9-18, they do not ask the court to construe the term "channel" and I will not do so. I am not convinced that construction of the term "channel" is necessary to resolve the parties' dispute, which relates to identifying where the channel forms in the accused products, that is, the channel region, as opposed to the channel itself.

Plaintiff also would have the court specifically define the channel region as the area between the source and drain regions, as the court did in Acer. All but two of the independent claims of the '463 patent describe the channel region as being "between" the source and drain regions. Figure 6H also labels the space between the source and drain regions as the channel region. However, it seems unnecessary to construe the term channel region as meaning the area located between the source and drain regions, when independent claims 1, 5, 12 and 13 of the patent specify that the channel region is between the source and drain regions. Construing channel region to include this same language would make the explicit limitation in claims 1, 5, 12 and 13 superfluous. Further, because claims 8 and 14 do not state that the channel region is between the source and drain regions, construing channel region more specifically may add an unintended limitation to claims 8 and 14. Finally, although Figure 6H depicts the channel region between the source and drain regions,

the specification makes clear that this is only a preferred embodiment of the invention. Golight, 355 F.3d at 1331 ("limitations from the specification are not to be read into the claims").

Plaintiff's proposed construction of "channel region" would include the vertical path that the electrical current takes from the source region to the channel and then back up to the drain region. Defendants contend that the channel region consists only of the bottom portion of the area that runs along the gate electrode where the channel is formed. According to defendants, the channel region in the accused products is the AL layer, a narrow layer (about 20 nanometers thick) of high-quality semiconductor material immediately above the gate insulation layers. The AL layer is not in contact with the source and drain regions because a separate protective layer (the AH layer) lies between the AL layer and the source and drain regions. Although plaintiff agrees that the accused products have both an AL and AH layer, it contends that nothing in the '463 patent limits the channel region to one layer and that together, the AH and AL layers constitute the channel region in the accused products.

I agree with plaintiff that nothing in the claim language or specification indicates that the channel region should be limited to one layer of semiconductor material. I am not persuaded by defendants' argument that the patent specification's reference to a semiconductive *layer* (singular) means that the channel region can never consist of two *layers*

(plural). Neither the patent claims nor the specification includes such a limitation. The patent also does not define the extent of the area making up the channel region. However, as the court concluded in Acer, it seems apparent that the channel region must at least include the channel itself. The parties agree that the channel is *at least* a layer of semiconductor material along the gate insulating layer that is rendered conductive by the gate electrode. It also is undisputed that when a voltage is applied to the gate electrodes of a thin film transistor, electric charge flows from the source region through the channel region to the drain region. Therefore, as the court did in Acer, I will construe the term channel region to mean an area that includes but is not limited to the channel.

Defendants attempt to distinguish the channel region in the accused products on the grounds that the AH layer, which is the layer in contact with the source and drain regions, is a lower quality semiconductor material that adds resistance and degrades the performance of the thin film transistor. However, it is undisputed that in the accused products, current flows through both the AH and AL layer from the source region to the drain region. Whether that current is slowed or impeded by an intermediate layer is irrelevant. Nothing in the '463 patent requires the claimed channel region to transmit current without an intermediate layer degrading the overall performance. In fact, the specification does not contain any discussion of the differences between a single layer and a multiple layer channel region. If the patent intended the claimed channel region to maximize current flow or

conductivity by using only one high quality layer of material in the channel region, it would have contained some discussion on the matter. Also irrelevant is defendants' claim that manufacturing the AL layer takes significantly more time than manufacturing the AH layer. The patent is silent with respect to the desired speed at which the channel region should be manufactured.

In sum, I decline to limit the term "channel region" by adding performance and manufacturing related requirements not claimed by the patent. Therefore, plaintiff is entitled to summary judgment with respect to whether the accused products satisfy the requirement in claims 1-7 and 12-13 that the channel region be in contact with the source and drain regions.

2. Construction of "between"

Related to the discussion of channel region is the meaning of the term "between" in claims 1, 5, 12 and 13. Defendants argue that if the channel region is to be "between" the source and drain regions, it must be bordered or surrounded directly by those regions. In other words, all three regions must be co-planar. Therefore, according to defendants, a channel region located below the source and drain regions is not "between" them. Plaintiff asserts correctly that this construction adds a limitation not specified in the '463 patent.

Nothing in the patent claims or specification indicates that the channel region has to be in the same plane as the source and drain regions. Although the only embodiment contained in the specification shows the source, drain and channel regions in the same plane (see Figure 6H), that is not necessarily the only allowable embodiment of the claim. Defendants point out that because only claims 1, 5, 12 and 13 disclose a channel region between the source and drain regions, those claims require a particular configuration of the source, drain and channel regions. Defendants are correct. These claims require a channel region located between the source and drain regions, unlike claims 8 and 14, which disclose only a semiconductor film having at least source, drain and channel regions. However, the requirement in claims 1, 5, 12 and 13 that the channel region be between the source and drain regions does not mean that the channel region must be directly beside or coplanar with the source and drain regions.

An object positioned below two other objects also may be between them. As plaintiff points out, an extension cord running from a wall-mounted television to an electrical outlet near the baseboard below also runs between the television and outlet, regardless whether it dips below both objects. The terms are not mutually exclusive. The parties agree that common definitions of the word between include "from one to the other of," "in the space that separates," "in an intermediate position in relation to two other objects" and "filling the space limited by two objects." This is consistent with the way in which the thin film

transistor operates. It is undisputed that when a voltage is applied to the gate electrodes of a thin film transistor, electric charge flows from the source region through the channel region to the drain region. In this sense, the channel region lies between the source and drain regions because it is in an intermediate position with respect to the source and drain regions along the same current path. Therefore, I will not limit the term "between" to meaning that the objects at issue must be co-planar.

Even assuming that only the AL layer comprises the "channel region" in the accused products, a reasonable jury could conclude from this only that the AL layer lies between the source and drain regions. It is undisputed that when the thin film transistor is turned on in the accused products, current flows from the source region through the AH layer to the AL layer, then back through the AH layer on its way to the drain region. Because the AL layer is in an intermediate position in relation to the source and drain regions along the current path, the AL layer is between the source and drain regions. Therefore, plaintiff is entitled to summary judgment with respect to the question whether the accused products satisfy the requirement in claims 1, 5, 12 and 13 that the accused channel region be located between the source and drain regions.

3. Construction of "semiconductor film"

Defendants contend that the term "semiconductor film" means a single layer of semiconductor material with source, drain and channel regions. However, for the reasons discussed above, nothing in the patent claims or specification requires the source, drain and channel regions to be located in a single layer or co-planar to one another. Although the only embodiment contained in the specification shows the source, drain and channel regions in a single layer (see Figures 6C and 6H), that is not necessarily the only embodiment of the claim. In fact, it is undisputed that at the time of the patented invention, it was known to those of ordinary skill in the art that there were multiple designs for thin film transistors, including ones that have the source and drain in the same layer as the channel and others that have the source and drain in a different layer.

Although the parties do not agree whether the single layer and multiple layer designs function differently, nothing in the patent indicates that this is an important distinction. For example, defendants contend that a multiple layer design insures that there are no contaminants between the source, drain and channel regions and that a single layer design requires the use of ion implantation or diffusion to form source and drain regions in the same semiconductor film, a process that degrades semiconductor materials and results in lower conductivity. However, as plaintiff points out, the patent specification does not

mention contaminants or their effect on the thin film transistor and says nothing about whether a single layer improves the performance of the thin film transistor.

Finally, defendants cite the prosecution history of the '463 patent in support of their argument that the semiconductor film disclosed in the '463 patent is a single layer. In 1997 and 1999, the patent examiner rejected the pending claims of the '463 patent as obvious over various references, including Matsumura, which disclose a channel region located in one semiconductor layer and source and drain regions located in a second, separate layer above the channel layer. However, the examiner never mentioned a "semiconductor film" in the various rejection letters. Further, it is undisputed that during the '463 patent prosecution, plaintiff did not distinguish Matsumura by claiming that the channel region in plaintiff's application was limited to channel regions on the same plane (or co-planar) as the source and drain regions. In a 1997 declaration, Yamazaki identified a transistor "in accordance with the present invention" that had source, drain and channel regions in a single layer of semiconductor material. However, that one statement does not show that plaintiff intended the '463 patent to embody *only* single layer semiconductor films.

It is undisputed that the thin film transistors in defendants' accused products comprise a semiconductor with source, drain and channel regions. Given this fact, a reasonable jury could conclude only that the accused products satisfy the element of claims 8, 9, and 14 requiring the claimed thin film transistor to have "a semiconductor film having

at least a source, drain and channel region." Therefore, plaintiff is entitled to summary judgment on the question whether defendants' products satisfy this element of claims 8, 9 and 14.

5. Construction of "junction"

All of the asserted claims require that the source and drain regions form "junctions" with the channel region. The parties do not agree about what kind of understanding a person of ordinary skill in the art would have had about the term junction as it is used in the '463 patent. Rexnord, 274 F.3d at 1342 (language must be construed as it would have been understood by one of ordinary skill in relevant art, given context and other patent claims). Defendants contend that at the time of the alleged '463 patent invention, people of ordinary skill in the art classified particular interfaces as either junctions or ohmic contacts on the bases of their electrical characteristics. Therefore, they propose construing junctions to mean only rectifying (or non-ohmic) interfaces between two different regions. Plaintiff contends that junction is a term of art used to refer to many different kinds of interfaces or electrical characteristics between different regions, including rectifying interfaces, non-rectifying interfaces, ohmic interfaces and non-ohmic interfaces. In its view, the plain and ordinary meaning of the term should apply: an intersection or interface between two different semiconductor regions, the place where two regions contact each other or come together.

As an initial matter, defendants argue that because many of the asserted claims disclose "junctions in contact," defining a junction generally as the place where two regions contact each other would render the term superfluous. I disagree. The place or point of contact between two objects is different from the state or condition of being "in contact."

Although various portions of the '463 patent claims refer to interfaces between the source and channel semiconductor regions as "junctions" and use the term junction to describe NI, PI and PN interfaces, neither the claims nor the specification further defines this term. Although it is not entirely clear from the undisputed facts whether NI, PI and PN interfaces are always non-ohmic, it does not matter. If the term "junction" is construed broadly to cover all types of contacts, it would make sense for the patent to be specific when it was discussing specific types of non-ohmic junctions. Defendants rely heavily on the fact that the patent specification includes one reference to the conductive layers making "ohmic contact" with the semiconductor layer, but the term is used in a completely different setting from that in the asserted claims. Nothing in the patent claims or specification requires a junction to always be a rectifying or non-ohmic interface. The broader definition also is consistent with that found in the technical literature cited by the parties. Finally, the "admissions" of Yamazaki and Lucovsky cited by defendants are ambiguous at best. Yamazaki definitely defines ohmic contacts only in the context of a different patent (the '636 patent). Lucovsky also discusses ohmic contacts and junctions in the context of the

'636 patent. Although initially he seems to state that junctions and ohmic contacts are completely different types of interfaces, he later explains that the two terms are not mutually exclusive and that a semiconductor junction is formed at the interface where two regions of different conductivity type are in contact with one another.

I will adopt plaintiff's proposed construction of the term "junction": an intersection or interface between two different semiconductor regions, the place where two regions contact each other or come together. Although the parties disagree whether the accused channel region forms a non-ohmic or ohmic contact with the source and drain regions, their dispute is irrelevant given the meaning of junction. Because it is undisputed that the accused channel and source and drain regions are semiconductor regions with different conductivity, a junction forms where the regions contact one another. Therefore, plaintiff is entitled to summary judgment on the question whether the accused products satisfy the requirement in claims 1-4, 8-12 and 14 that the channel region forms junctions with the source and drain regions. However, because the parties disagree whether the source and drain regions in the accused products form NI or N^+I junctions with the channel region, it will be left for the jury to resolve this question. As a result, I am unable to determine whether the accused products satisfy the requirement in claims 5 and 13 that these junctions be PI or NI.

C. Non-Single Crystal Semiconductor Material

In the context of plaintiff's summary judgment motion, the parties dispute the meaning of "non-single crystal semiconductor material" in claims 1 and 5. Although plaintiff's motion is limited to those claims, this term appears in claims 1, 5, 12 and 13. Specifically, the patent claims disclose "source and drain regions comprising a non-single crystal semiconductor material doped with a recombination center neutralizer." Plaintiff would have the court adopt the definition provided in the specification and adopted by the court in Acer for the '941 patent: "a semi-amorphous semiconductor, an amorphous semiconductor or a mixture thereof." Defendants contend that the term should be limited to semi-amorphous semiconductor material.

The patent specification is explicit in defining "non-single crystal semiconductor material" as including amorphous or semi-amorphous semiconductor material or a mixture of the two. Defendants argue that the court should disregard this instruction because the specification explains that amorphous semiconductor materials cannot be used for the source and drain regions, explicitly describes only semi-amorphous semiconductor material, disparages amorphous and other semiconductor materials and fails to disclose a single embodiment of source and drain materials made of amorphous or other semiconductor materials. The crux of defendants' argument is that the specification teaches only a method of manufacturing a semi-amorphous semiconductor and identifies the non-single crystal

semiconductor as the starting material, preventing the patent from covering products consisting of amorphous semiconductors.

According to the only embodiment contained in the specification, the starting material undergoes a structural change that is induced by localized heating (the step depicted in Figure 6G) and results in a final product (the source and drain regions) made of semi-amorphous semiconductor material. Defendants assert that because the specification indicates that this process can be used where the non-single crystal semiconductor is amorphous or some other semiconductor material, the final product is always semi-amorphous semiconductor material, necessitating that the "non-single crystal semiconductor material" be semi-amorphous semiconductor material. I disagree.

The specification illustrates the formation of a thin film transistor in which starting semiconductor material is converted into semi-amorphous semiconductor material through the application of a current. However, the specification states explicitly that the process described clarifies "the manufacturing method of the present invention and its advantages in the case where the non-single crystal semiconductor 7 is the semi-amorphous semiconductor." This leaves open the possibility that the non-single crystal semiconductor could be a different type of semiconductor.

Defendants point out that the specification goes on to state that

> Also in the case where the non-single crystal semiconductor 7 is an amorphous semiconductor or a mixture of the semi-amorphous semiconductor and the amorphous semiconductor, it can be formed by the above-described method.

The specification later states:

> Even if the non-single crystal semiconductor 7 is the amorphous semi-conductor or the mixture of the semi-amorphous and the amorphous semiconductor, the semi-amorphous semiconductor S2 is formed to have the same construction as in the case where the non-single crystal semiconductor 7 is the semi-amorphous one.

I agree that the second statement seems to imply that amorphous or mixed semiconductor material results in a final semi-amorphous semiconductor. However, the patent abstract describes the invention as

> A semiconductor device which has a non-single crystal semiconductor layer formed on a substrate and in which the non-single crystal semiconductor layer is composed of a first semiconductor region formed primarily of non-single crystal semiconductor and a second semi-conductor region formed primarily of semi-amorphous semiconductor. The second semi-conductor region has a higher degree of conductivity than the first semiconductor region so that a semi-conductor element ray [sic: may] be formed.

The resulting semiconductor regions, including the more conductive region, are not limited to semi-amorphous semiconductor material. Therefore, there is no ground for limiting the meaning of non-single crystal semiconductor to semi-amorphous semiconductor. Various statements in the specification emphasize the point that a non-single crystal semiconductor can be an amorphous or a semi-amorphous one or a combination of the two. It seems implausible that the specification would define non-single crystal semiconductor material

initially as including a variety of materials but later intend that term to refer to only one type of semiconductor material. If plaintiff had intended to describe the source and drain regions in the patent claims as limited to semi-amorphous material, it would have said so, rather than using the broader definition of the term "non-single crystal semiconductor material."

Equally unpersuasive are defendants' arguments that plaintiff disavowed a broad definition of the claim term by including only one embodiment disclosing a final semi-amorphous semiconductor product or making disparaging remarks about the properties of amorphous semiconductors. At most, these factors indicate plaintiff's strong preference for semi-amorphous semiconductors. However, as plaintiff notes, preferred embodiments cannot be used to limit claim language intended to have a broader effect. Innova/Pure Water, Inc. v. Safari Water Filtration Systems, 381 F.3d 1111, 1117 (Fed. Cir. 2004) (even when patent describes only single embodiment, otherwise broader claims will not be read restrictively unless patentee has demonstrated clear intention to limit claim scope in that manner.)

Because I construe non-single crystal semiconductor material to mean "a semi-amorphous semiconductor, an amorphous semiconductor or a mixture thereof," it is irrelevant whether the accused products contain semi-amorphous or only amorphous semiconductor material. Therefore, plaintiff is entitled to summary judgment on the

question whether defendants' products satisfy the non-single crystal semiconductor element of claims 1 and 5.

D. Intrinsic Amorphous Semiconductor Material

The parties disagree over the meaning of "intrinsic" as it is used in claims 5 and 13, which both recite "said channel region comprising an intrinsic amorphous silicon semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof." The parties generally agree that "intrinsic" material is "undoped" in some fashion. However, they disagree about the extent to which amorphous semiconductor material can be doped, if at all. Neither side cites support in the specification for its proposed constructions, relying instead on expert testimony to support its version of what one of ordinary skill in the art would have understood the term to mean in the '463 patent.

Plaintiff would limit the claim term to mean "amorphous silicon semiconductor material not intentionally doped with an efficient dopant." According to plaintiff, when an efficient dopant is added to semiconductor material in the source, drain or channel region of a thin film transistor, the material changes into an N-type or P-type conductivity. Plaintiff defines efficient dopants as almost always being phosphorus or boron because these additives substantially affect the conductivity type of a semiconductor material, that is, they

make the material highly conductive. Plaintiff asserts that inefficient dopants like recombination center neutralizers do not substantially affect the semiconductor's type of conductivity.

Adopting the construction found by the court in Acer, defendants contend that intrinsic amorphous silicon semiconductor material is "a pure or near pure layer of amorphous silicon semiconductor material that previously has not been doped." They contend that whether a dopant is efficient depends greatly on the process condition and the host material. According to defendants, hydrogen can have a substantial effect on conductivity in amorphous silicon, whereas phosphorus or boron alone cannot substantially affect the conductivity of the material unless hydrogen or another recombination center neutralizer is present. Defendants also point out that the common definition of intrinsic is "undoped." Plaintiff asserts that the dictionary references cited by defendants fail to take into account the type of material involved, that is, amorphous semiconductor material.

The patent does not mention efficient or inefficient dopants or boron or phosphorus dopants. Moreover, it is not entirely clear from the parties' submissions what understanding a person of ordinary skill in the art would have had with respect to the term "intrinsic" amorphous silicon semiconductor material. Therefore, at trial, the jury will be asked to decide to what a person of ordinary skill in the art would have understood at the time of the invention about the extent to which an "intrinsic" amorphous semiconductor material can

be doped, if at all. Once that question is resolved, the court will determine how the term should be construed in light of the claims language, specification and understanding of a person of ordinary skill in the art. Also apparently in dispute and a potential issue for trial is the composition of the amorphous semiconductor material in the channel region of the accused products.

II. ANTICIPATION AND OBVIOUSNESS ANALYSIS

A. Legal Standard

Under 35 U.S.C. § 282, patents are presumed valid. A party challenging the validity of a patent has the burden to make its showing by clear and convincing evidence. Helifix Ltd. v. Blok-Lok, Ltd., 208 F.3d 1339, 1346 (Fed. Cir. 2000); Connell v. Sears Roebuck & Co., 722 F.2d 1542, 1549 (Fed. Cir. 1983). A patent is anticipated "if the invention was patented or described in a printed publication in this or a foreign country . . . more than one year prior to the date of the application for patent in the United States." 35 U.S.C. § 102(b). To prove anticipation, defendants must show that "all aspects of the claimed invention were already described in a single reference." Scripps Clinic & Research Foundation v. Genentech, Inc., 927 F.2d 1565, 1576- 77 (Fed. Cir. 1991); see also In re Trans Texas Holdings Corp., 498 F.3d 1290, 1300 (Fed. Cir. 2007) (invalidity counterclaims of both independent and dependent claims may rise and fall on failure to

teach a single limitation). Generally, the facts relevant to this finding are the reference claimed to be prior art and evidence of what the reference meant to persons of ordinary skill in the field of the invention. Id. The anticipation inquiry proceeds on a claim-by-claim basis. Sinisar Corp. v. DirectTV Group, Inc., 523 F.3d 1323, 1334 (Fed. Cir. 2008).

A court may invalidate a patent for obviousness "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." 35 U.S.C. § 103(a). "Determining obviousness requires considering whether *two or more* pieces of prior art could be combined, or a single piece of prior art could be modified, to produce the claimed invention." Comaper Corp. v. Antec, Inc., 596 F.3d 1343, 1351-52 (Fed. Cir. 2010) (emphasis added). In performing this analysis, the question is usually whether a person having ordinary skill in the art would have found some teaching, suggestion or motivation to combine or modify the prior art references. Pfizer, Inc. v. Apotex, Inc., 480 F.3d 1348, 1362 (Fed. Cir. 2007). The Unites States Supreme Court has held that the prior art need not include a specific teaching to solve the particular problem at issue, emphasizing that "[c]ommon sense teaches . . . that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." KSR International Company v. Teleflex Inc., 550 U.S. 398, 420 (2007);

see also Ortho-McNeil Pharm., Inc. v. Mylan Labs., Inc., 520 F.3d 1358, 1364-65 (Fed. Cir. 2008) (noting that the test, flexibly applied, remains an important tool in an obviousness analysis).

Although "obviousness" is a question of law, underlying factual questions are relevant to the analysis, including: (1) the scope and content of the prior art; (2) differences between the prior art and the claims at issue; and (3) the level of ordinary skill in the pertinent art. KSR, 550 U.S. at 406 (citing Graham v. John Deere Co. of Kansas City, 383 U.S. 1, 17-18 (1966)); PharmaStem Therapeutics, Inc. v. ViaCell, Inc., 491 F.3d 1342, 1359-60 (Fed. Cir. 2007). "[S]econdary considerations [such] as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented." KSR, 550 U.S. at 406.

As an initial matter, the parties dispute the level of ordinary skill in the art at the time of the issuance of the '463 patent and the relevant field of the invention for the '463 patent. Defendants contend that the skill level is a Masters of Science degree in either electrical engineering, material science or a related field and three years of experience in semiconductor fabrication or a Ph.D. in those fields. Plaintiff contends that the skill level is a bachelor's degree in electrical engineering, chemistry, materials science, mechanical engineering, chemical engineering or a related field with two to three years' experience working with thin film transistor technology. Although it will be up to the jury to decide these issues at trial,

I note that with respect to invalidity, both Dr. Fair and Dr. Liu have said that under either proposed level of skill and field of art, their opinions would be the same. Therefore, the parties' dispute about the state of the art at the time the '463 patent was issued is not material.

B. Sakamoto: Anticipation and Obviousness

The parties dispute whether Sakamoto contains all of the limitations of the '463 patent, so as to make the '463 patent invalid as anticipated. Plaintiff denies that it does, saying that Sakamoto fails to disclose the limitation of "recombination center neutralizer" found in all of the asserted claims of the '463 patent and an "intrinsic channel region" found in claims 2, 5, 9 and 13 of the '463 patent. Defendants deny that any limitation is missing and argue in the alternative that any missing limitation would have been obvious to one of ordinary skill in the art.

1. "Recombination center neutralizer" limitation

All of the asserted claims of the '463 patent require that the source, drain and channel regions consist of semiconductor material doped with "a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof." Although

Sakamoto does not expressly disclose this limitation, defendants argue that it is disclosed inherently.

A patent does not disclose an element inherently unless the element is "necessarily present and a person of ordinary skill in the art would recognize its presence." Crown Operations International, Ltd. v. Solutia, Inc., 289 F.3d 1367, 1377 (Fed. Cir. 2002); see also Continental Can Company USA, Inc. v. Monsanto Company, 948 F.2d 1264, 1268-69 (Fed. Cir. 1991) (holding same). "Inherency 'may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" Id. (quoting Continental Can, 948 F.2d at 1269). "In general, a limitation . . . is inherent and in the public domain if it is the 'natural result flowing from' the explicit disclosure of the prior art." Schering Corp. v. Geneva Pharmaceuticals, 339 F.3d 1373, 1379 (Fed. Cir. 2003) (internal citations omitted). Because the '463 patent is presumed valid, defendants bear the evidentiary burden of establishing that the recombination center neutralizer limitation was inherent. Id.

In support of their inherency argument, defendants contend that when Sakamoto was filed, it was known in the art that undoped amorphous silicon was not a "suitable" material for thin film transistors and that amorphous silicon thin film transistors would not function properly or effectively unless they contained hydrogen or a halogen as a recombination center neutralizer. Defendants cite several references showing that amorphous silicon

contains dangling bonds that act as recombination centers, which trap charged particles and reduce the conductivity of the semiconductor material. Citing various references, defendants' expert, Dr. Fair, states that "[e]arly TFT devices using pure amorphous silicon showed no field effect response, which made it fatal for TFTs" and "a TFT in which the source and drain regions contain hydrogen or a halogen, but the channel does not, still cannot function." Dkt. #211, ¶¶ 214, 216. He also states that "dangling bonds rendered pure amorphous silicon unusable in semiconductor devices." Id., ¶ 216.

Plaintiff points out that Sakamoto is silent about the way in which the source, drain and channel regions are formed, making it impossible to know whether a recombination center neutralizer is necessarily present. Plaintiff's expert, Dr. Liu, offers the opinion that thin film transistors constructed from pure amorphous silicon without a recombination center neutralizer work, even if they are less effective. Dkt. #195 at 34. Liu bases her opinion on the fact that it was *possible* to manufacture pure amorphous silicon by evaporation and sputtering without hydrogen or a halogen and that this silicon was used in thin film transistors that were tested by researchers. It is unclear how far this opinion will take plaintiff, but a reasonable jury could conclude that such devices have some level of functionality.

Plaintiff points out that Fair avers that a recombination center neutralizer is necessary to create an "effective" or "suitable" thin film transistor. Plaintiff interprets this statement

as a concession that although undoped amorphous silicon transistors may be less effective, they can still function, albeit poorly. I disagree. As previously discussed, Fair makes it clear elsewhere in his report that his position is that pure amorphous silicon thin film transistors are ineffective and unusable, indicating that they do not function at all. Plaintiff also points to a statement made by Fair in his report that it was well known that amorphous silicon formed through either evaporation or sputtering or silane decomposition without N or P type dopants could function as the semiconductor layer of a thin film transistor, dkt. #215, Exh. 45, ¶ 314, but I do not read this statement as conceding the point that thin film transistors with pure, unhydrogenated amorphous silicon are functional. In context, Fair seems to be discussing hydrogenated amorphous silicon, not pure amorphous silicon.

In a separate inherency argument, defendants assert that when Sakamoto was published, it was known that amorphous silicon could not be doped effectively to have N-type or P-type conductivity unless its dangling bonds were neutralized with hydrogen or a halogen. They argue that because Sakamoto discloses an amorphous silicon thin film transistor with source and drain regions formed by doping with N-type or P-type impurities, that transistor necessarily had to include a recombination center neutralizer comprised of hydrogen or a halogen. Because plaintiff's expert disputes all of these assertions, these questions will be left for the jury to decide at trial.

In sum, although I agree with plaintiff that the inherency of a missing element cannot be established merely by showing that a device would be preferable or would function better with that element, factual disputes do not allow me to decide as a matter of law whether Sakamoto inherently discloses source, drain and channel regions with a recombination center neutralizer. It is not clear how effective an amorphous silicon thin film transistor is without the addition of a recombination center neutralizer, if it is effective at all, and what was known about its effectiveness in 1978 when Sakamoto was published. If, as plaintiff contends, such thin film transistors existed and were merely less effective, defendants cannot establish that Sakamoto inherently disclosed a recombination center neutralizer. However, if amorphous silicon thin film transistors not doped with a recombination center neutralizer were not made in 1978 because they were ineffective, a reasonable jury could conclude that Sakamoto inherently discloses a recombination center neutralizer.

Given the material issues of fact remaining in dispute, the parties' motions for summary judgment will be denied with respect to the question whether the recombination center neutralizer element in the '463 patent was anticipated by Sakamoto.

2. Obviousness of using recombination center neutralizers

Although it remains disputed whether Sakamoto anticipated the claims of the '463 patent, defendants argue that it would have been obvious to one of ordinary skill in the art

at the time of the invention of the '463 patent to dope the amorphous silicon of the source, drain and channel regions with hydrogen or a halogen given (a) the knowledge of one of ordinary skill in the art; (b) the admitted prior art; and (c) the prior art references disclosing the use of a recombination center neutralizer for amorphous silicon thin film transistors. In support of their argument, defendants point out that plaintiff admitted in JP '974, the '463 patent file history and the deposition of Dr. Yamazaki that using hydrogen, a halogen or a mixture of both as a recombination center neutralizer for amorphous silicon was known prior art at the time of the alleged invention. Defendants also cite numerous prior art references that disclose the use of hydrogen or a halogen as a recombination center neutralizer. They argue that these references show that a known solution existed for the known problem of dangling bonds in amorphous silicon. KSR, 550 U.S. at 419-20 ("One of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution.").

In response to defendants' motion for summary judgment, plaintiff contends that 1) Sakamoto is not analogous to the '463 patent because it is not part of the same field of endeavor; 2) there was never a reason to combine Sakamoto with other references disclosing a recombination center neutralizer; and 3) one of ordinary skill in the art would not have had a reasonable expectation of success in combining Sakamoto with any other reference.

The only prior art relevant to a consideration of obviousness under 35 U.S.C. § 103 is "analogous art." Comaper Corp. v. Antec, Inc., 596 F.3d 1343, 1351 (Fed. Cir. 2010) (citing Wang Labs., Inc. v. Toshiba Corp., 993 F.2d 858, 864 (Fed. Cir. 1993). "Two criteria are relevant in determining whether prior art is analogous: '(1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the inventor's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved.'" Id. (quoting In re Clay, 966 F.2d 656, 658-59 (Fed. Cir. 1992)).

The parties dispute whether Sakamoto is in the same field of endeavor as the '463 patent. Sakamoto discloses devices used for making a compact integrated circuit memory on a conductive silicon substrate, whereas the '463 patent discloses an amorphous or semi-amorphous thin film transistor on a glass substrate. Plaintiff contends that Sakamoto's disclosure relates to a device that is designed and manufactured differently from the thin film transistors used in integrated circuit memory; defendants contend that the semiconductor devices that Sakamoto discloses may be used in other applications, just as the thin film transistor of the '463 patent can be used in memory applications.

In addition, the parties dispute whether Sakamoto is reasonably pertinent to the particular problems addressed by the '463 patent, which is directed to a semiconductor with a higher degree of photoelectric conversion efficiency, comprising elements formed with

higher integration density, that can be manufactured easily and at low cost. The question is complicated by Sakamoto's statement that he was attempting to reduce the size of the semiconductor pellet on which integrated circuit memory is mounted and to increase the performance and capacity of such memory.

It simply is not clear from the evidence adduced by the parties whether Sakamoto is part of the same field of endeavor as the '463 patent or whether Sakamoto is related at all to the problems addressed by the '463 patent. Although defendants cite portions of the '463 patent specification that make general references to "memory," it is not clear whether the memory being discussed is the same type disclosed in Sakamoto. I conclude that defendants have not shown that they are entitled to summary judgment on their claim that the '463 patent claims are rendered obvious by Sakamoto. Accordingly, it is unnecessary to address plaintiff's other challenges to defendants' obviousness claim.

3. "Intrinsic" channel region

Claims 2, 5, 9 and 13 of the '463 patent require the channel region either to comprise intrinsic amorphous silicon or to be of an intrinsic conductivity type. As discussed in this court's previous order on infringement of the '463 patent, the parties dispute the proper construction of the term "intrinsic." Defendants contend that intrinsic amorphous silicon semiconductor material is "a pure or near pure layer of amorphous silicon semiconductor

material that previously has not been doped." On the other hand, plaintiff would limit the term to "amorphous silicon semiconductor material not intentionally doped with an efficient dopant."

> Sakamoto does not use the term intrinsic. However, it discloses the following:
>
> > [E]ither the first polysilicon or amorphous silicon film 203 or 204 that is formed on the thick silicon oxide film containing effective dopants is used as a source or drain, respectively; and *similarly*, a part of the surface of the either polysilicon or amorphous silicon film 205 is used as a channel region.

(Emphasis added). Plaintiff asserts that this is an express disclosure of a *doped* channel region. It uses the term "similarly," meaning that the amorphous silicon film of the channel region also contains effective dopants. Alternatively, plaintiff contends, because Sakamoto is silent with respect to the doping and conductivity type of the channel region, that region could be intrinsic or non-intrinsic.

Defendants contend that because Sakamoto describes the channel region as simply formed in the amorphous silicon film without any disclosure of doping, it expressly discloses an *undoped* or intrinsic channel region. Defendants' expert, Dr. Fair, avers that one of ordinary skill in the art at the time would understand "effective dopants" to mean N-type or P-type impurities that would result in a N-type or P-type conductivity for the source and drain regions. Defendants also point out that Figure 2 of Sakamoto depicts source and drain regions with dots, which Fair avers illustrates the effective dopants, and a channel region

without dots, indicating no effective dopants. Plaintiff disagrees with defendants' interpretations of Sakamoto because the reference is silent with respect to the meaning of "effective dopants" and how the dots are used in Figure 2.

Given the parties' dispute over the meaning of the claim term "intrinsic" and what constitutes an effective dopant (i.e., the effect on conductivity type), it is not possible to determine as a matter of law whether Sakamoto discloses an "intrinsic" channel region as that term is used in the '463 patent. However, I can conclude from reading Sakamoto that the claimed channel region is not doped with "effective dopants." The reference clearly identifies the source and drain regions as having effective dopants and does not include such a limitation with respect to the channel region. The use of dots in the source and drain regions but not the channel region in Figure 2 is consistent with this construction. The use of the word "similarly" is ambiguous at best; it certainly does not make clear that the channel region must contain effective dopants. Therefore, defendants' motion for summary judgment will be denied with respect to whether Sakamoto anticipates the intrinsic channel region disclosed in the '463 patent claims. The jury will need to decide underlying factual issues related to the meaning of intrinsic and effective dopants before it can be determined whether Sakamoto anticipates the '463 patent with respect to an intrinsic channel region.

D. Kasmerski and JP '663 and '664: Anticipation

Plaintiff asserts that it is entitled to summary judgment with respect to defendants' claims that the '463 patent is invalid as anticipated by Kasmerski and JP '663 and '664. It contends that defendants improperly combine two or more embodiments in the Kasmerski and JP '663 and '664 references to find all of the limitations in the asserted claims of the '463 patent. In support of its argument, plaintiff cites Net Money IN, Inc. v. Verisign, Inc., 545 F.3d 1359, 1370-71 (Fed. Cir. 2008), in which the Court of Appeals for the Federal Circuit emphasized the

> importance of the requirement that the reference describe not only the elements of the claimed invention, but also that it describe those elements "arranged as in the claim:"
>
> > To anticipate a claim, a single prior art reference must expressly or inherently disclose each claim limitation. . . . But disclosure of each element is not quite enough—this court has long held that '[a]nticipation requires the presence in a single prior art disclosure of all elements of a claimed invention arranged as in the claim.

Id. at 1371 (quoting Finisar Corporation v. DirecTV Group, Inc., 523 F.3d 1323, 1334 (Fed. Cir. 2008) (internal citation omitted)). The court held that "unless a reference discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations arranged or combined in the same way as recited in the claim, it

cannot be said to prove prior invention of the thing claimed and, thus, cannot anticipate under 35 U.S.C. § 102." Id.

1. Kasmerski

Defendants contend that Kazmerski anticipates all of the asserted claims of the '463 patent, but plaintiff denies this, asserting that Kazmerski fails to disclose a gate insulating film comprising a nitride, which is present in all of the asserted claims. Plaintiff points out that Figure 6.16 of Kasmerski shows an *oxide* gate insulating film. Defendants respond with a citation to an earlier paragraph in Kazmerski that states that "work by Madan et al." used a silicon *nitride* insulating layer. Defendants contend that Kazmerski makes it clear that silicon nitride is a suitable gate insulating film that would be arranged as the insulating layer between the gate electrode and the semiconductor film (or a-Si:H).

I agree with plaintiff that defendants actually are making an obviousness argument in arguing that Kazmerski discloses all of the elements of the asserted '463 patent claims. Kazmerski does not comment on the suitability of silicon nitride as an insulating layer. Instead, Kazmerski merely notes that Madan used "a thin film of amorphous Si_3N_4 (~1-3 *J-tm* thick). . . as the insulating layer, and then gate voltages of ~ 50 V were able to produce a modulation of ~ 10^3 in the drain current." Kazmerski says nothing to suggest that he believed that Madan's device was successful or even suitable. Indeed, Kazmerski goes on to

state that "[m]ore recently, L. A. Goodman [76] at RCA Laboratories has succeeded in fabricating a-Si:H TFTs using a metal-oxide semiconductor (MOS) structure (see Fig. 6.16)," implying that Goodman's device is preferable to that disclosed in Figure 6.16 and consistent with it. Accordingly, plaintiff is entitled to summary judgment on the question whether the '463 patent claims are invalid as anticipated by Kazmerski.

2. JP '663 and '664

All of the asserted claims of the '463 patent disclose a channel region comprising amorphous silicon. In its motion for summary judgment, plaintiff contends that defendants' anticipation argument fails because no single embodiment or claim in either application discloses all of the elements of the '463 patent claims. In arguing that an amorphous silicon channel region is anticipated in JP '663 and '664, defendants rely on a specific embodiment in the applications to find all of the elements of the '463 patent except for "non-monocrystalline semiconductor." For that element, defendants rely on an introductory paragraph in those applications, entitled "Detailed Description of Invention," which explains that the invention generally relates to a "non-monocrystalline semiconductor" in which at least a part of the channel region is "amorphous or polycrystalline." The introductory section also states that the "present invention makes it possible to sufficiently minimize the concentration of recombination centers . . . in a non-monocrystalline (polycrystalline or

amorphous) material." Defendants also note that claim 1 of each application discloses a channel region formed with a non-monocrystalline semiconductor.

Plaintiff takes issue with the fact that the definition of non-monocrystalline semiconductor appears only in an introductory section and not in the embodiment that contains the other elements of the '463 patent claims. Plaintiff further notes that unlike the '463 patent, the embodiment does not teach the use of amorphous silicon in a completed device. Relying on Liu's expert report, plaintiff contends that the channel region disclosed in the JP '663 and '664 embodiment is polycrystalline silicon, not amorphous silicon. Plaintiff fails to make Liu's reasoning clear in properly proposed findings of fact but a review of her report shows that she reached this conclusion because the embodiments of JP '663 and '664 disclose high fabrication techniques that would crystalize any amorphous silicon semiconductor channel material. Dkt. #195 at 21.

However, not only do the introductory sections of the JP '663 and '664 specifications generally define non-monocrystalline semiconductor material as polycrystalline or amorphous silicon, they also specify that the claimed invention includes a channel region that is at least in part "amorphous or polycrystalline." This disclosure could apply to the later stated embodiments even if it appears in a general section of the specification describing the claimed invention. In fact, the Court of Appeals for the Federal Circuit has held in the context of claims construction that "[w]hen a patent thus describes the features

of the 'present invention' as a whole, this description limits the scope of the invention." TiVo, Inc. v. EchoStar Communications Corp., 516 F.3d 1290, 1300 (Fed. Cir. 2008) (quoting Verizon Servicess Corp. v. Vonage Holdings Corp., 503 F.3d 1295, 1308 (Fed. Cir. 2007)).

Thus, even though defendants draw limitations from both the general description of the invention and an embodiment, this does not mean that the limitations are not arranged or combined in the same way as those recited in the '463 patent claims. JP '663 and '664 generally disclose an "invention" that includes an amorphous or polysilicon channel region. Therefore, it stands to reason that an embodiment of that invention would include the same options for the composition of the channel region unless the embodiment specifically states otherwise. Although plaintiff contends that one of ordinary skill in the art would understand the first embodiment of JP '663 and '664 to disclose a completed device with only a polysilicon channel region because of the heating methods employed, it has not proposed findings of fact sufficient to establish this point or to put the issue in dispute. Because there is evidence that the embodiment disclosed can be either partly amorphous or partly polycrystalline, that embodiment may anticipate the '463 patent claims. Accordingly, plaintiff's motion for summary judgment on defendants' claim that the '463 patent is invalid as anticipated by JP '663 and '664 is denied. Whether those references anticipate the '463 patent claims will remain an issue for trial.

E. Matsumura and LeComber: Obviousness

Defendants claim that the '463 patent is invalid as obvious in light of Matsumura and LeComber because Matsumura discloses all of the limitations in the asserted claims of the '463 patent except a silicon nitride gate insulating film, which LeComber discloses. Defendants contend that although the '463 patent examiner considered obviousness in light of both Matsumura and LeComber, plaintiff and Dr. Matsumura have admitted since then that it would have been obvious to combine these two references and the Supreme Court's 2007 decision in KSR now compels a finding of invalidity.

1. Plaintiff's admissions

Defendants rely on two admissions allegedly made by plaintiff during SEL I. In SEL I, plaintiff filed a motion for reconsideration of an inequitable conduct ruling regarding its '636 patent. It argued that because the patent office had considered Matsumura and LeComber, which had the same disclosures as Canon, the allegedly concealed portions of Canon were cumulative of those references and therefore, did not have to be disclosed. In support of its argument, plaintiff submitted a declaration from Dr. Matsumura, who averred that silicon nitride could replace silicon oxide as the gate insulator in his device when LeComber is considered.

Although I agree that these "admissions" may prove relevant to the obviousness inquiry because they might indicate what was understood by one of ordinary skill in the relevant field of the invention, they are not dispositive on that issue. As plaintiff points out, nothing in the cited portions of the motion for reconsideration establishes that it would have been obvious of one of ordinary skill in the art to combine Matsumura with LeComber in 1980. Similarly, in his 1998 declaration, Dr. Matsumura does not make any statements with respect to the state of the art or the reasons why it would have been obvious to combine Matsumura and LeComber. Further, as plaintiff asserts, as an inventor, Matsumura's "personal expectations are not conclusive of an ordinary skilled artisan's reasonable expectations." Amgen Inc. v. F. Hoffman-LA Roche Ltd., 580 F.3d 1340, 1363 (Fed. Cir. 2009) (cautioning against determining obviousness by inquiring into what inventors would have known or would likely have done faced with particular references). Finally, both "admissions" relate to the '636 patent, which although similar, has not been shown to have exactly the same disclosures, purpose or resulting device as the '463 patent claims.

2. KSR obviousness test

Traditionally, the Court of Appeals for the Federal Circuit has held that a defendant attempting to prove obviousness had to show "a motivation or suggestion" to combine separate elements of prior art and "a reasonable expectation of success" in doing so.

Boehringer Ingelheim Vetmedica, Inc. v. Schering-Plough Corp., 320 F.3d 1339, 1354 (Fed. Cir. 2003); Teleflex, Inc. v. Ficosa North American Corporation, 299 F.3d 1313, 1334 (Fed. Cir. 2002). However, in KSR International Company v. Teleflex, Inc., 550 U.S. 398, 419 (2007), the Supreme Court cautioned that the "obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents." Although the Court observed that "it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does," id. at 418, it made it clear that "neither the particular motivation nor the avowed purpose of the patentee controls;" "[w]hat matters is the objective reach of the claim," id. at 419. The Court noted that it often will be necessary "for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." Id. at 418.

Since KSR, the Federal Circuit has considered the revised obviousness inquiry and confirmed that where "the content of the prior art, the scope of the patent claim, and the level of ordinary skill in the art are not in material dispute, and the obviousness of the claim

is apparent in light of these factors, summary judgment is appropriate." E.g., Boston Scientific Scimed, Inc. v. Cordis Corp., 554 F.3d 982, 992 (Fed. Cir. 2009) (quoting KSR, 127 S. Ct. at 1745-46); Sundance, Inc. v. DeMonte Fabricating Ltd., 550 F.3d 1356, 1366 (Fed. Cir. 2008) (quoting same); Asyst Techs., Inc. v. Emtrak, Inc., 544 F.3d 1310, (Fed. Cir. 2008) (quoting same). However, the court of appeals has continued to emphasize teaching, suggestion and motivation as relevant inquiries. E.g., Procter & Gamble Company v. Teva Pharmaceuticals USA, Inc., 566 F.3d 989, 997 (Fed. Cir. 2009) ("patents are not barred just because it was obvious 'to explore a new technology or general approach that seemed to be a promising field of experimentation, where the prior art gave only general guidance as to the particular form of the claimed invention or how to achieve it.'") (quoting In re O'Farrell, 853 F.2d 894, 903 (1988)); Boston Scientific, 554 F.3d at 991 (applying KSR and also finding that "one of ordinary skill in the art would have been motivated to combine" two embodiments in one prior art reference). Therefore, although I agree with defendants that the Supreme Court has warned against a rigid application of the "teaching, suggestion or motivation" test (commonly known as the "TSM test"), that decision does not require this court to reach a conclusion contrary to that of the Board of Patent Appeals and Interferences as a matter of law.

During the '463 patent prosecution, the board determined that the patent examiner had not given a convincing explanation for his conclusion that Matsumura and LeComber

would have rendered the '463 patent claims obvious. However, in making this determination, the board considered the relative content and context of Matsumura and LeComber; the possibility that a person of ordinary skill in the art even could have applied the insulator disclosed in LeComber to the type of device disclosed by Matsumura; and general knowledge surrounding silicon nitride insulators and their suitability in devices having the specific type of structure and purpose disclosed in Matsumura. These remain appropriate and relevant inquiries, even after KSR.

In any event, because the parties dispute material issues of fact about obviousness of the '463 patent in light of Matsumura and LeComber, these factual questions must be resolved by the jury at trial. Although the parties do not dispute the content of Matsumura and LeComber or the scope of the '463 patent, they dispute whether one of ordinary skill in the art would have thought to substitute a silicon nitride insulator for a silicon oxide insulator in a thin film transistor, knowing the properties and relative benefits of the two substances (otherwise known as objective evidence of obviousness). KSR, 550 U.S. at 417 (prior art combination more likely obvious where the "inventor" "'simply arranges old elements with each performing the same function it had been known to perform' and yields no more than one would expect from such an arrangement") (internal citation omitted). As previously discussed, the parties in this case disagree about what was known about the benefits and functioning of silicon nitride insulators at the time. Therefore, defendants'

motion for summary judgment with respect to the question whether the '463 patent is invalid as obvious in light of Matsumura and LeComber is denied.

F. Remaining Obviousness Issues

Defendants also move for summary judgment on their claim that the '463 patent is invalid as obvious in light of Matsumura and Sakamoto. However, for the reasons explained above, material issues of fact remain in dispute with respect to both of these references, the relevant field of invention, the relevant skill level in the art and whether substituting silicon nitride for silicon oxide in the Matsumura device would have been predictable, routine or even possible.

Finally, I note that in response to defendants' motion for summary judgment on invalidity of the '463 patent, plaintiff raises arguments regarding secondary obviousness considerations. Given the parties' factual disputes with respect to obviousness, it is unnecessary to discuss these secondary considerations at this point.

ORDER

IT IS ORDERED that

1. The motion for summary judgment filed by defendants Samsung Electronics Company, Ltd., S-LCD Corporation, Samsung Electronics America, Inc., Samsung

Telecommunications America, LLC and Samsung Mobile Display Co., Ltd. on noninfringement of the '463 patent, dkt. #201, is DENIED.

2. Plaintiff Semiconductor Energy Laboratory Company, Ltd.'s motion for summary judgment on infringement of the '463 patent, dkt. #202, is GRANTED with respect to the following questions:

a. Whether the accused products satisfy the requirement in claims 1-7 and 12-13 that the channel region be "in contact" with the source and drain regions;

b. Whether the accused products satisfy the requirement in claims 1, 5, 12 and 13 that the accused channel region be located "between" the source and drain regions;

c. Whether the accused products satisfy the element of claims 8, 9, and 14 requiring the claimed thin film transistor to have "a semiconductor film having at least a source, drain and channel region";

d. Whether the accused products satisfy the requirement in claims 1-4, 8-12 and 14 that the channel region form junctions with the source and drain regions; and

e. Whether the accused products satisfy the non-single crystal semiconductor element of claims 1 and 5.

3. Plaintiff's motion for summary judgment on infringement is DENIED with respect to the other elements of claims 1-14 of the '463 patent. Remaining as issues for trial on infringement are whether the accused products satisfy the requirements in claims 5 and 13

of the '463 patent that the channel region (1) form PI or NI junctions with the source and drain regions and (2) is comprised of an intrinsic amorphous silicon semiconductor material.

4. Defendants' motion for summary judgment on whether the '463 patent is invalid as obvious in light of Matsumura and LeComber or Sakamoto is DENIED.

5. Plaintiff's motion for summary judgment on defendants' claim that the '463 patent is invalid as anticipated by Kazmerski is GRANTED and defendants' claim is DISMISSED.

6. Plaintiff's motion for summary judgment on defendants' claim that the '463 patent is invalid as anticipated by JP '663 and '664 is DENIED.

7. The following questions relating to anticipation and obviousness of the '463 patent remain for trial:

a. Whether the '463 patent is anticipated or rendered obvious by Sakamoto;

b. Whether JP '663 and '664 anticipates the '463 patent; and

c. Whether the combination of Matsumura and LeComber or Matsumura and Sakamoto render the '463 patent claims obvious.

8. The parties' motions for summary judgment on inequitable conduct and other affirmative defenses of all the patents in suit and on anticipation and obviousness of the '402, '516 and '937 patents will be addressed in a separate order.

Entered this 7th day of May, 2010.

BY THE COURT:
/s/
BARBARA B. CRABB
District Judge